STABILIZIRAN USMERNIK 1-30V 0-3A

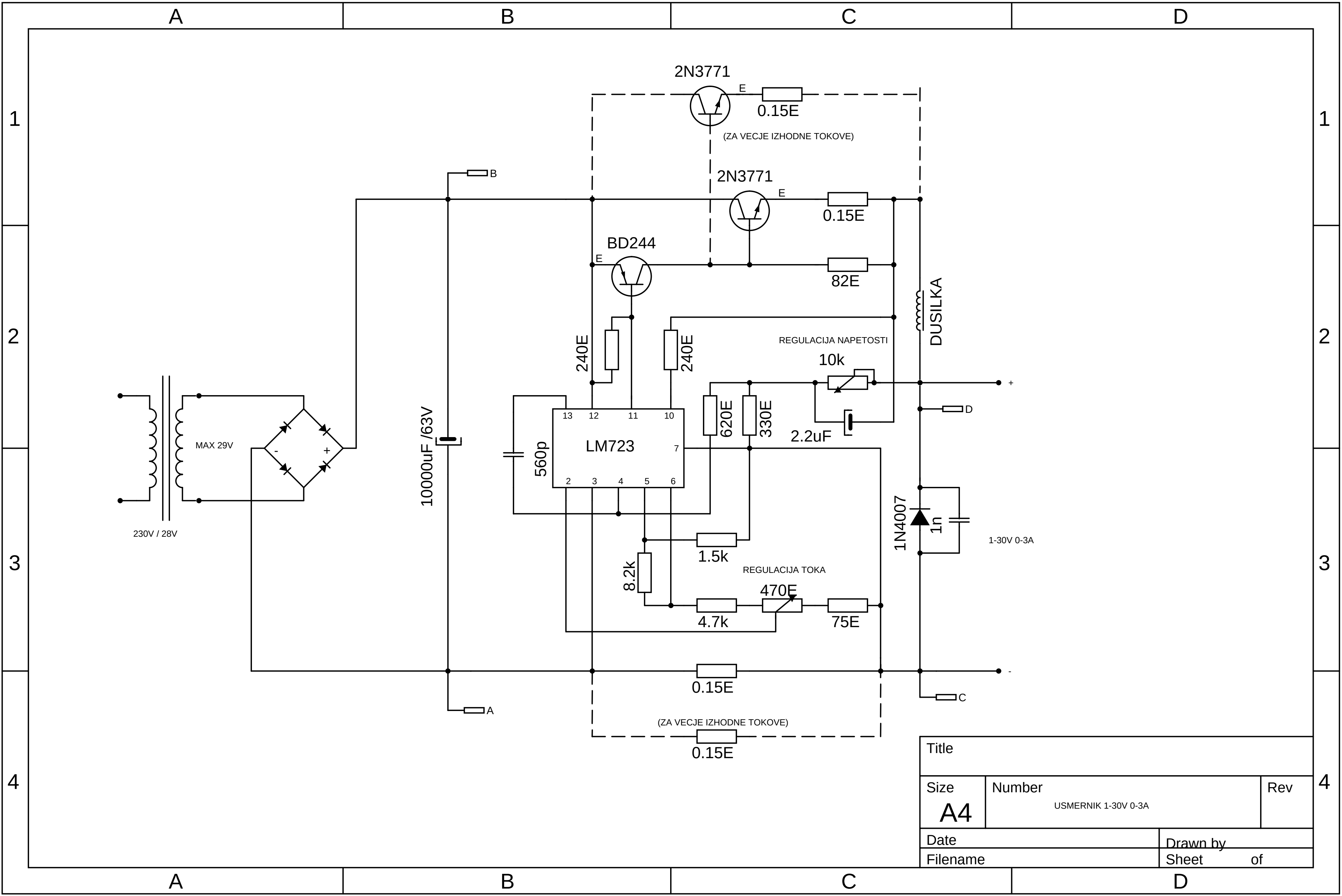
Ker mi v domaci delavnici vcasih ni bil dovolj en usmernik sem se odlocil za izdelavo še enega. Edino uporabljeno integrirano vezje je LM723 Gre za napetostni regulator ,ki se pojavlja na trgu ze od leta 1968 !!.Podatek ,da se je "obdrzal" na trgu vec kot 32 let prica ,da gre za uporaben element. Je tudi poceni in dobavljiv v vsaki trgovini z elektroniko. Vec o samem vezju je opisano v prilogi.

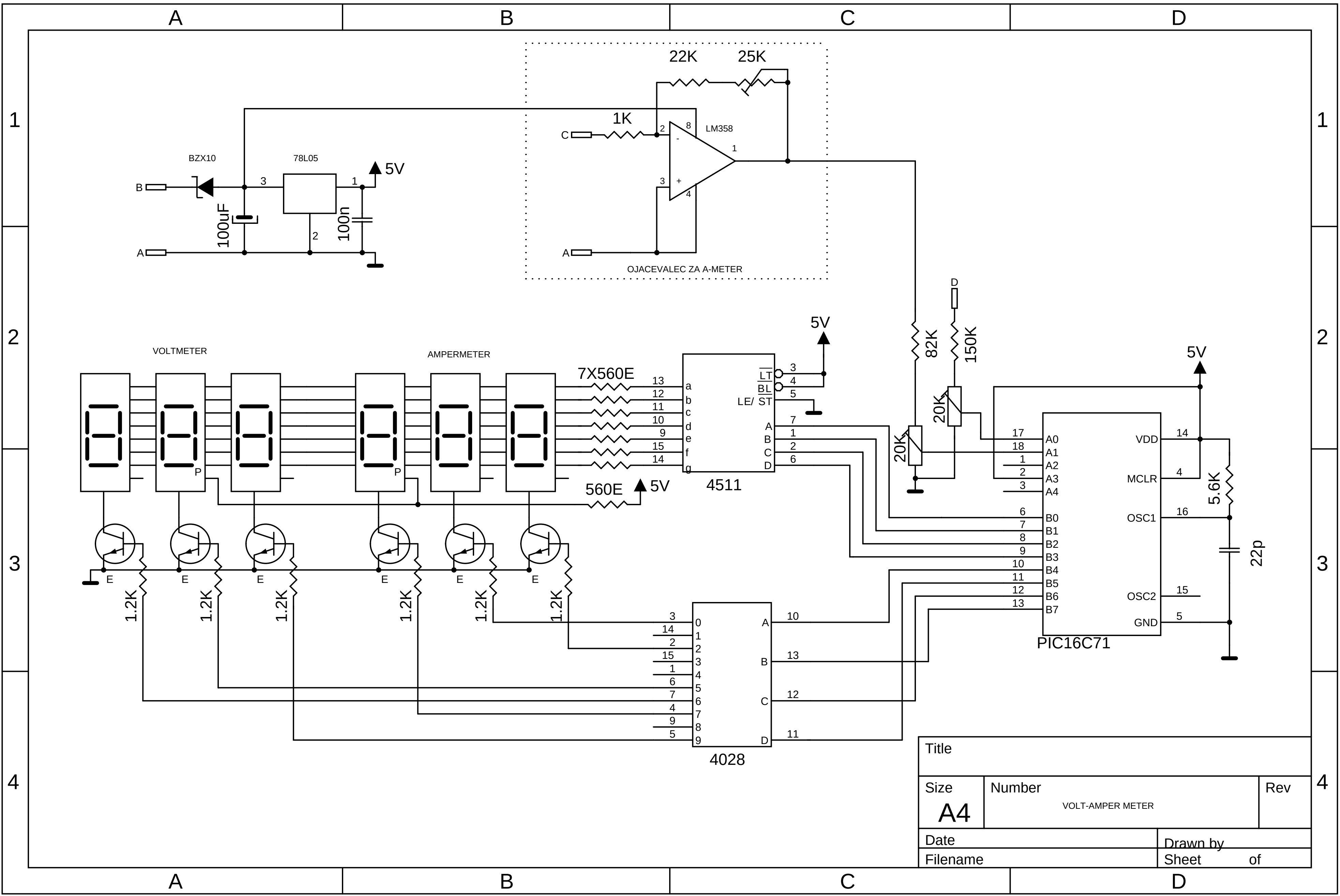
Izdelava:
Usmernik sem naredil na prilozenem tiskanem vezju. (sam sem naredil dvojni usmernik zato je tudi TIV predvideno za dva usmernika)
Na samem TIV ni predviden diodni mostic ter elektrolitski kondenzator 10 000 uF (sam sem uporabil oba elemeta za montazo na ohišje) prav tako je potrebno na hladilno rebro zmontirati izhodni transistor 2N3771 (ali podobnega) zašcitna dioda 1N4007 ter kondenzator 1n se prilota neposredno na izhodne sponke.

DIGITALNI V-A METER

Nujno potreben instrument na takem usmerniku je tudi volt in amper meter. Ustrezni ze narejeni instrumenti se sicer dajo kupit.Sam sem ga naredil s PIC16C71 (PIC16C711)
Kratek opis:
Za meritev sta uporabljena 2 AD vhoda (RA0,RA1)
Z prvim vhodom se meri napetost (max prikaz je 51.0V korak po 0.2V)
Z drugim vhodom se meri tok (max prikaz je 2.55A korak po 10mA)
RA3 je referencni vhod (z njim se definira referenca vhoda RA0 ter RA1)
Sam sem uporabil referenco 5V torej sem RA3 zvezal na +5V Ce bi kdo zelel nizjo referencno napetost mora narediti uporovni delilnik (tiskano vezje je pripravljeno). Za prikaz sem uporabil 6 displejev s skupno katodo. Na vezju je potrebno z zicko narediti povezave za vklop decimalnih pik (glej nacrt)
Za merjenje toka sem naredil ojacevalec z LM358. (na drugi tiskovini)
Vse skupaj se direktno napaja z usmernika. V koliko se uporbi transformator z sekundarno napetostjo vec kot 24 V (ce je na 1.elektrolitu vec kot 30V je potrebno zaporedno z napajanjem zvezati 10V 1W zener diodo (glej nacrt)
Sicer lahko pride do pregrevanja in izklapljanja stabilizatorja 78L05
Pine na PIC-u sem "razširil" s pomocjo dveh poceni CMOS-ov (4511 ter 4028 podroben opis v prilogi.)

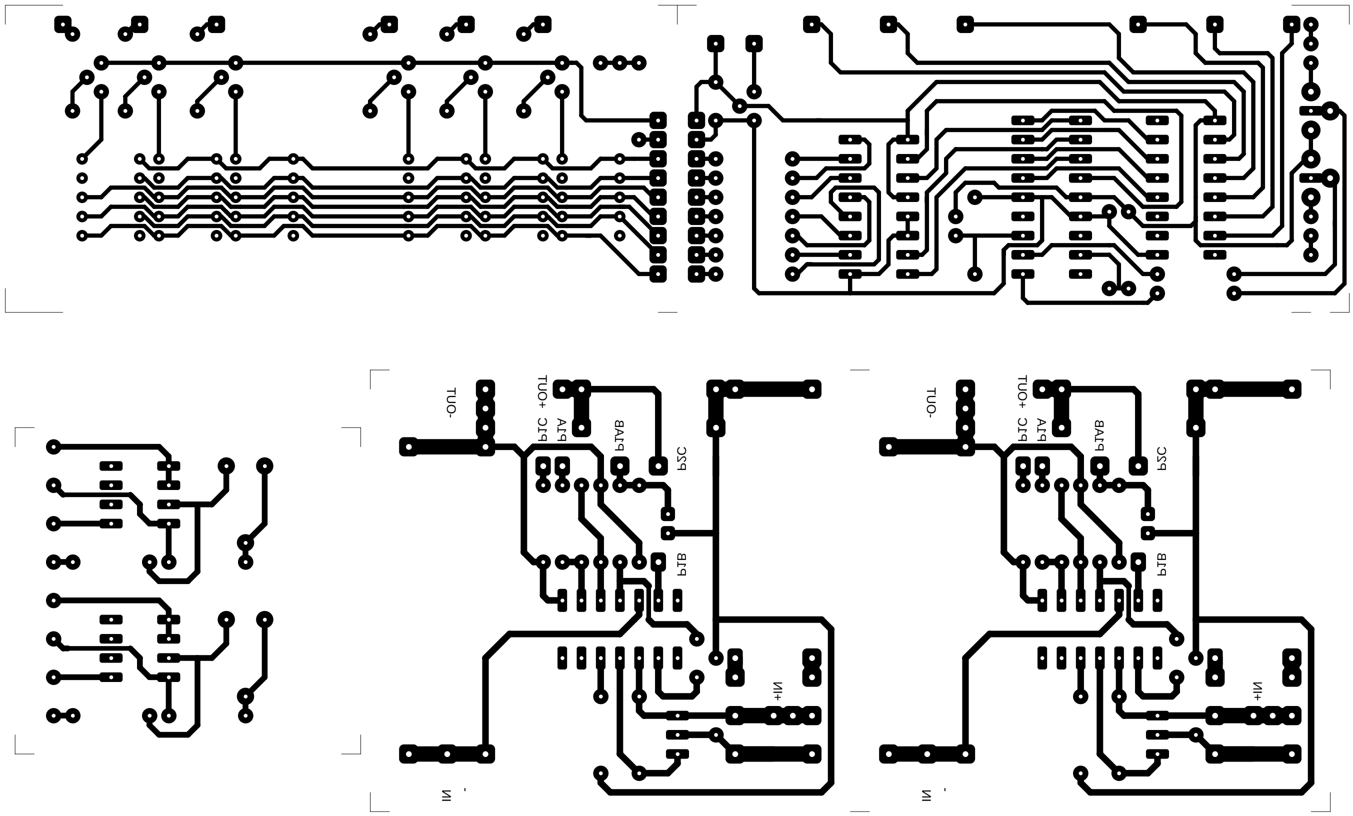
silvo.straser@lycos.com
silvo.straser@email.si

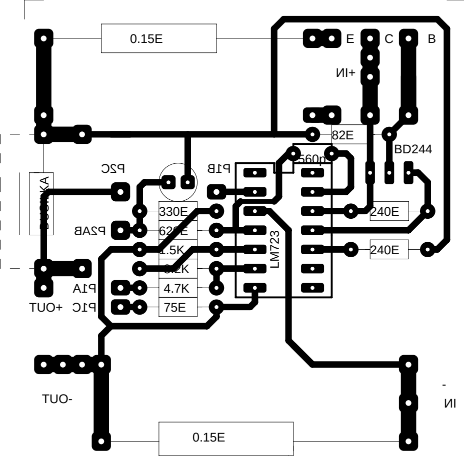

2N3771
E
0.15E
(ZA VECJE IZHODNE TOKOVE)
2N3771
E
0.15E
BD244
E
82E
DUSILKA
B
240E
240E
REGULACIJA NAPETOSTI
10k
+
D
2.2uF
620E
330E
LM723
13 12 11 10
7
2 3 4 5 6
560p
10000uF /63V
MAX 29V
230V / 28V
1N4007
1n
1-30V 0-3A
1.5k
REGULACIJA TOKA
8.2k
470E
4.7k
75E
-
0.15E
C
A
(ZA VECJE IZHODNE TOKOVE)
0.15E
Title
Size
A4
Number
USMERNIK 1-30V 0-3A
Rev
Date
Drawn by
Filename
Sheet of

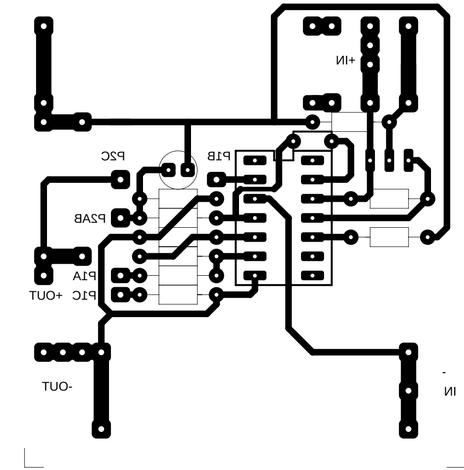


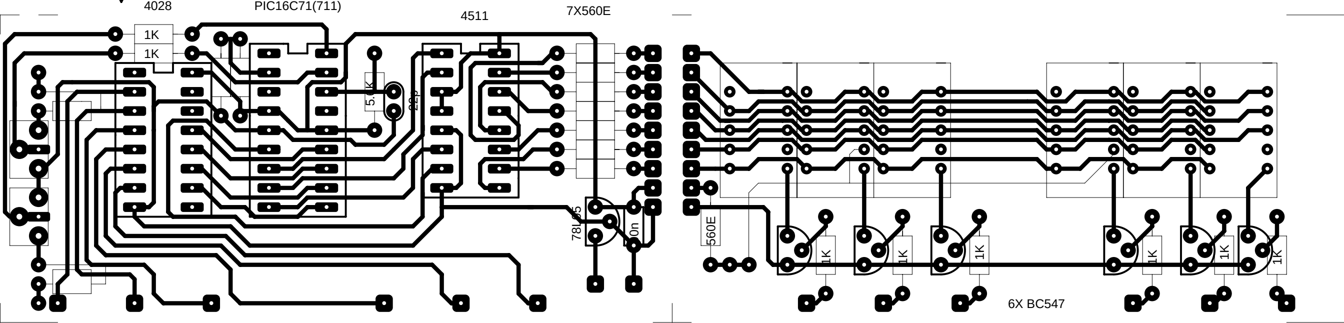
BZX10
78L05
5V
100uF
100n
22K
25K
1K
LM358
OJACEVALEC ZA A-METER
VOLTMETER
AMPERMETER
7X560E
560E
4511
LT
BL
LE/ ST
82K
150K
20K
PIC16C71
VDD
MCLR
OSC1
OSC2
GND
5.6K
22p
1.2K
4028
Title
Size
A4
Number
VOLT-AMPER METER
Rev
Date
Drawn by
Filename
Sheet
of

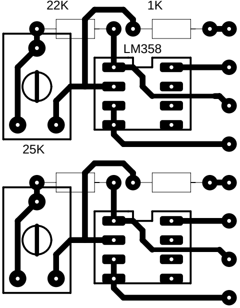
:02000000A62830
:0800080005288C00030E8D0099
:1000100083010B1910280D0E83008C0E0C0E0900A5
:100020007C209B1C16289B101B18632019200B1189
:100030000B289508031D2128950A12088038860090
:10004000080001301502031D2A28950A13080038FC
:1000500086000800023015020310D3328950A140893
:10006000D038860008000330150203 1D3C28950A8D
:100070000F083038860008000430150203 1D45289B
:10008000950A100850388600080095011108C038FC
:1000900086000800960197019801 8E008E080319CA
:1000A000080064308E02031C5728980A51286430D7
:1000B0008E070A308E02031C5F28970A59280A30DF
:1000C0000E07960008001A084A20822016088F00A2
:1000D00017089000180891001908 4A201608920085
:1000E000170893001808940 01B100800640064307F
:1000F0009C009C0B792808009D0B08009B143C3049
:100100009D000800960D16101B110A301602031CE4
:100110008C280A3096021B15970D17101B191714FF
:100120001B110A301702031C98280A3097021B156E
:10013000980D18101B191814080 00C308400800149
:10014000840A30300402031C9F28080064009D20AC
:10015000030166008316D330810001308800831 2CA
:1001600095019B01A0308B00413088003C309D0000
:10017000640088117620081564000819BC28090855
:100180009A008815762008156400081 9C428090803
:060190009 9001B14B828C1
:02400E00F73F7A
:00000001FF




0.15E
E
C
B
+IN
82E
BD244
560p
P2C
P1B
330E
620E
1.5K
4.7K
75E
LM723
240E
240E
P2AB
P1A
P1C
+OUT
-OUT
-
IN
0.15E


+IN
P2C
P1B
P2AB
P1A
P1C
+OUT
-OUT
-
IN

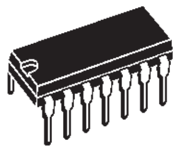

4028
PIC16C71(711)
4511
7X560E
1K
1K
5.6K
22p
78L05
560E
6X BC547
1K
1K
1K
1K
1K
1K


22K
1K
LM358
25K

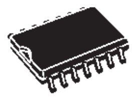
LM723

HIGH PRECISION VOLTAGE REGULATOR

- INPUT VOLTAGE UP TO 40V
- OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37V
- POSITIVE OR NEGATIVE SUPPLY OPERATION
- SERIES, SHUNT, SWITCHING OR FLOATING OPERATION
- OUTPUT CURRENT TO 150mA WITHOUT EXTERNAL PASS TRANSISTOR
- ADJUSTABLE CURRENT LIMITING



Plastic DIP-14

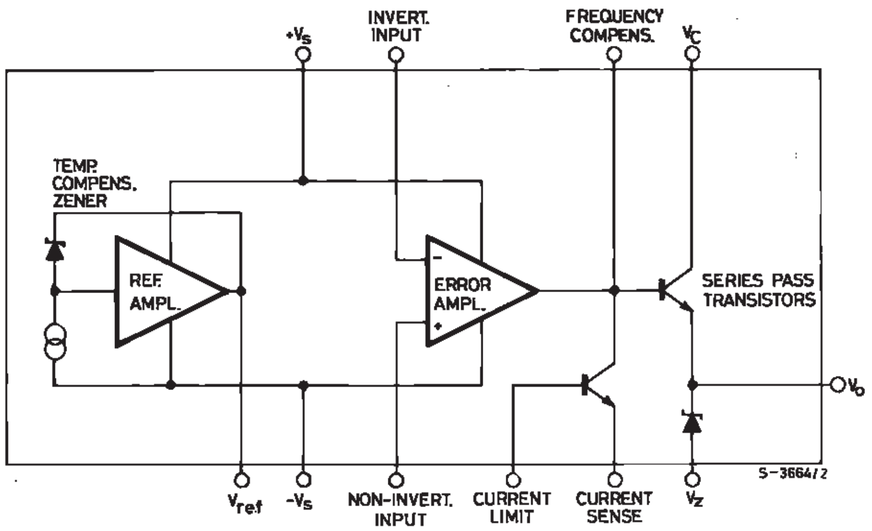


SO-14

DESCRIPTION

The LM723 is a monolithic integrated programmable voltage regulator, assembled in 14-lead dual in-line plastic and SO-14 micropackage. The circuit provides internal current limiting. When the output current excedes 150mA an external NPN or PNP pass element may be used. Provisions are made for adjustable current limiting and remote shut-down.

BLOCK DIAGRAM



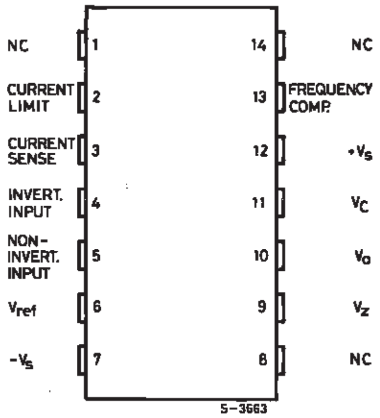
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		LM723	LM723C	
V_i	DC Input Voltage	40	40	V
ΔV_{i-o}	Dropout Voltage	40	40	V
I_o	Output Current	150	150	mA
I_{ref}	Current from V_{ref}	15	25	mA
T_{op}	Operating Temperature	-55 to 125	0 to 70	^oC
T_{stg}	Storage Temperature	-65 to 150	-65 to 150	^oC
T_j	Junction Temperature	150	125	^oC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Plastic DIP-14	SO-14	Unit
$R_{thj-amb}$	Thermal Resistance Junction-Ambient	Max	200	160	$^oC/W$

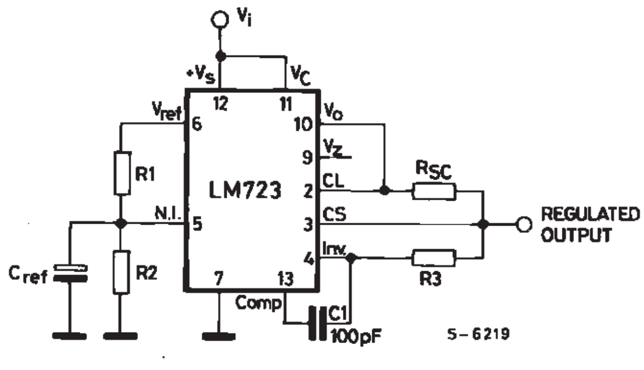
PIN CONNECTION (top views)



ORDER CODES

Type	Plastic DIP-14	SO-14
LM723 LM723C	LM723N LM723CN	 LM723CD

TEST CIRCUIT (pin configuration relative to the plastic package)



$V_i = 12V$
$V_o = 5V$
$I_o = 1mA$
$R_1/R_2 \leq 10K\Omega$

ELECTRICAL CHARACTERISTICS FOR LM723 (refer to the test circuits, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$\Delta V_o/\Delta V_i$	Line Regulation	V_i = 12 to 15V V_i = 12 to 40V V_i = 12 to 15V -55°C ≤ T_{amb} ≤ 125°C		0.01 0.02	0.1 0.2 0.3	% % %
$\Delta V_o/V_o$	Load Regulation	I_o = 1 to 50 mA I_o = 1 to 10 mA -55°C ≤ T_{amb} ≤ 125°C		0.03	0.15 0.6	% %
V_{REF}	Reference Voltage	I_{ref} = 160 µA	6.95	7.15	7.35	V
SVR	Supply Voltage Rejection	f = 100 Hz to 10 KHz C_{ref} = 0 f = 100 Hz to 10 KHz C_{ref} = 5 µF		74 86		dB dB
$\Delta V_o/\Delta T$	Output Voltage Drift				150	ppm/°C
I_{sc}	Output Current Limit	R_{sc} = 10Ω V_o = 0		65		mA
V_i	Input Voltage Range		9.5		40	V
V_o	Output Voltage Range		2		37	V
V_o-V_i			3		38	V
I_d	Quiescent Current	V_i = 30 V I_o = 0 mA		2.3	5	mA
K_{VH}	Long Term Stability			0.1		%/1000 hrs
e_N	Output Noise Voltage	BW = 100 Hz to 10 KHz C_{ref} = 0 BW = 100 Hz to 10 KHz C_{ref} = 5 µF		20 2.5		µV µV

ELECTRICAL CHARACTERISTICS FOR LM723C (refer to the test circuits, T_{amb} = 25 °C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$\Delta V_o/\Delta V_i$	Line Regulation	V_i = 12 to 15V V_i = 12 to 40V V_i = 12 to 15V 0°C ≤ T_{amb} ≤ 70°C		0.01 0.1	0.1 0.5 0.3	% % %
$\Delta V_o/V_o$	Load Regulation	I_o = 1 to 50 mA I_o = 1 to 10 mA 0°C ≤ T_{amb} ≤ 70°C		0.03	0.2 0.6	% %
V_{REF}	Reference Voltage	I_{ref} = 160 µA	6.8	7.15	7.5	V
SVR	Supply Voltage Rejection	f = 100 Hz to 10 KHz C_{ref} = 0 f = 100 Hz to 10 KHz C_{ref} = 5 µF		74 86		dB dB
$\Delta V_o/\Delta T$	Output Voltage Drift				150	ppm/°C
I_{sc}	Output Current Limit	R_{sc} = 10Ω V_o = 0		65		mA
V_i	Input Voltage Range		9.5		40	V
V_o	Output Voltage Range		2		37	V
V_o-V_i			3		38	V
I_d	Quiescent Current	V_i = 30 V I_o = 0 mA		2.3	4	mA
K_{VH}	Long Term Stability			0.1		%/1000 hrs
e_N	Output Noise Voltage	BW = 100 Hz to 10 KHz C_{ref} = 0 BW = 100 Hz to 10 KHz C_{ref} = 5 µF		20 2.5		µV µV

Figure 1 : Maximum Output Current vs. Voltage Drop.

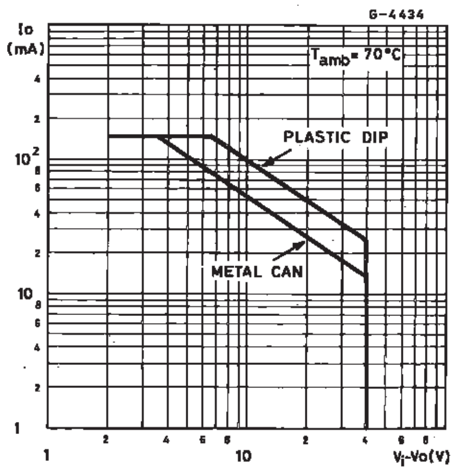


Figure 2 : Current Limiting Characteristics.

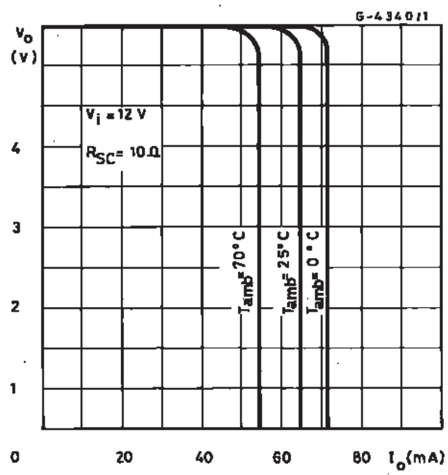


Figure 3 : Current Limiting Characteristics vs. Junction Temperature.

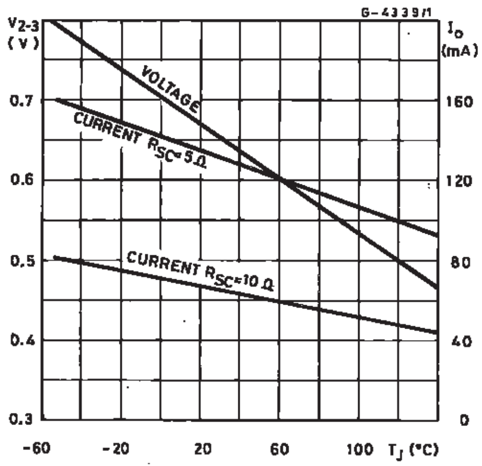


Figure 4 : Load Regulation Characteristics without Current Limiting.

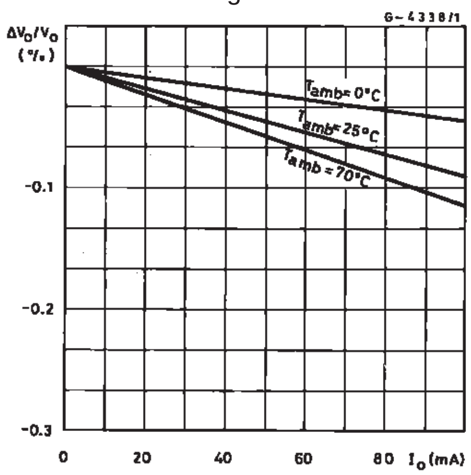


Figure 5 : Load Regulation Characteristics with Current Limiting.

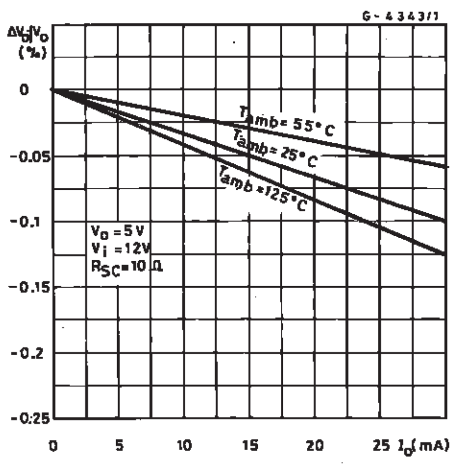


Figure 6 : Load Regulation Characteristics with Current Limiting

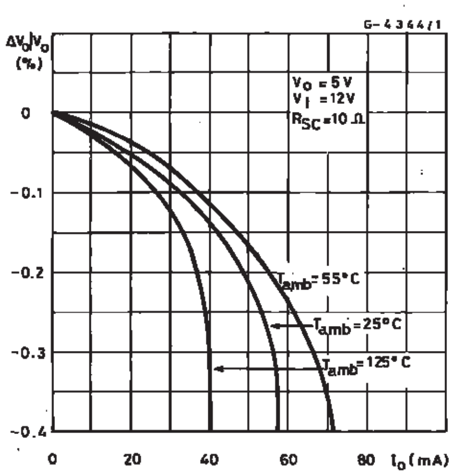


Figure 7 : Line Regulation vs. Voltage Drop.

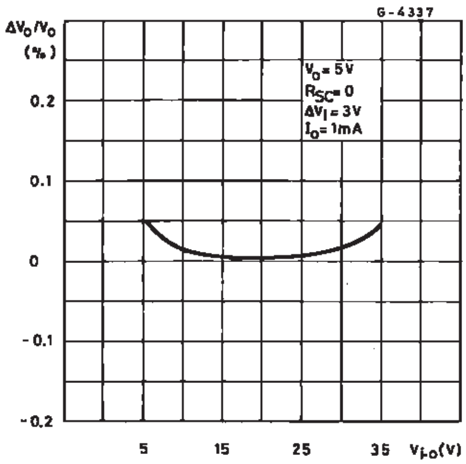


Figure 8 : Load Regulation vs. Voltage Drop.

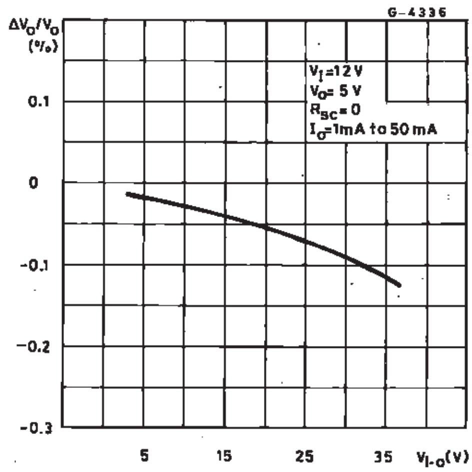


Figure 9 : Quiescent Drain Current vs. Input Voltage.

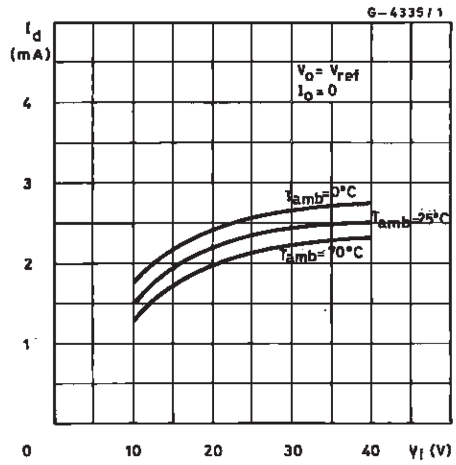


Figure 10 : Line Transient Response.

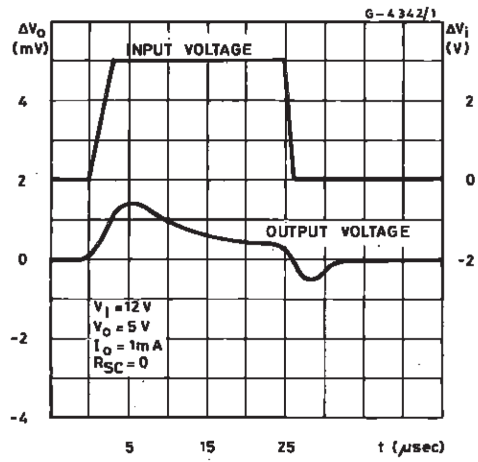


Figure 11 : Load Transient Response.

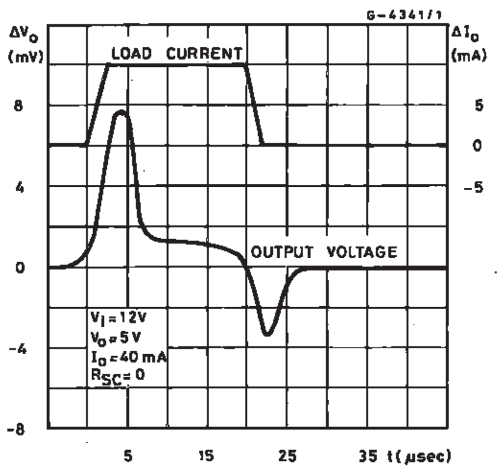


Figure 12 : Output Impedance vs. Frequency.

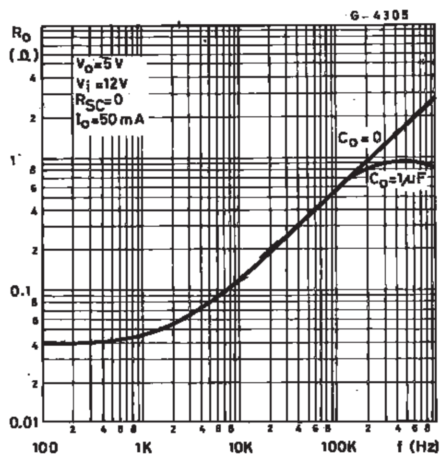


TABLE 1: Resistor Values (KΩ) for standard Output Voltages

Output Voltage	Applicable Figures	Fixed Output ± 5%		Output Adjustable ± 10% *		
		R1	R2	R1	P1	R2
+3	13, 16, 17, 18, 21, 23	4.12	3.01	1.8	0.5	1.2
+5	13, 16, 17, 18, 21, 23	2.15	4.99	0.75	0.5	2.2
+6	13, 16, 17, 18, 21, 23	1.15	6.04	0.5	0.5	2.7
+9	14, 16, 17, 18, 21, 23	1.87	7.15	0.75	1	2.7
+12	14, 16, 17, 18, 21, 23	4.87	7.15	2	1	3
+15	14, 16, 17, 18, 21, 23	7.87	7.15	3.3	1	3
+28	14, 16, 17, 18, 21, 23	21	7.15	5.6	1	2
+45	19	3.57	48.7	2.2	10	39
+75	19	3.57	78.7	2.2	10	68
+100	19	3.57	102	2.2	10	91
+250	19	3.57	255	2.2	10	240
-6**	15	3.57	2.43	1.2	0.5	0.75
-9	15	3.48	5.36	1.2	0.5	2
-12	15	3.57	8.45	1.2	0.5	3.3
-15	15	3.65	11.5	1.2	0.5	4.3
-28	15	3.57	24.3	1.2	0.5	10
-45	20	3.57	21.2	2.2	10	33
-100	20	3.57	97.6	2.2	10	91
-250	20	3.57	249	2.2	10	240

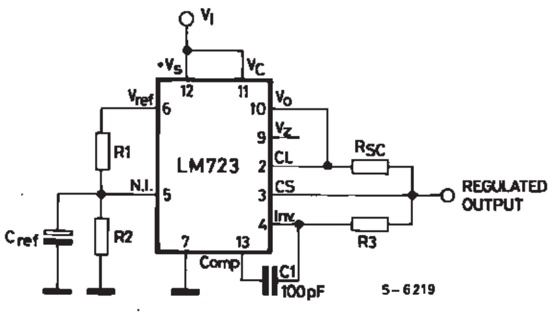
Note:
* Replace R1/R2 divider with the circuit of fig24.
** V+ must be connected to a +3V or greater supply.

TABLE 2: Formulae for Intermediate Output Voltages

Outputs from +2 to +7V Fig.13, 16, 17, 18, 21, 23 $V_O = [V_{ref} \times \frac{R_2}{R_1 + R_2}]$	Outputs from +4 to +250V Fig.19 $V_O = \left[\frac{V_{ref}}{2} \times \frac{R_2 - R_1}{R_1}\right]; R_3 = R_4$	Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$
Outputs from +7 to +37V Fig.14, 16, 17, 18, 21, 23 $V_O = [V_{ref} \times \frac{R_1 + R_2}{R_2}]$	Outputs from -6 to -250V Fig.15, 20 $V_O = \left[\frac{V_{ref}}{2} \times \frac{R_1 + R_2}{R_1}\right]; R_3 = R_4$	Foldback Current Limiting $I_{KNEE} = \left[\frac{V_O R_3}{R_{sc} R_4} \times \frac{V_{SENSE}(R_3 + R_4)}{R_{sc} R_4}\right]$ $I_{SHORT\ CKT} = \left[\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}\right]$

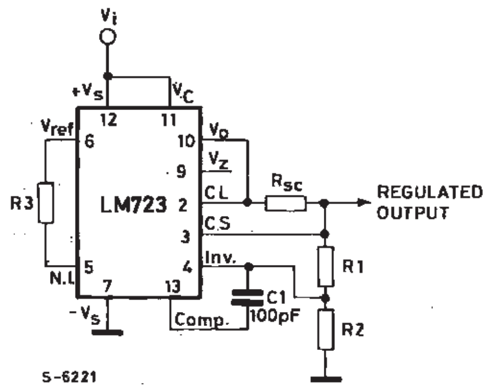
APPLICATION INFORMATION (pin numbers relative to the plastic package).

Figure 13 : Basic Low Voltage Regulator (V_o = 2 to 7V).



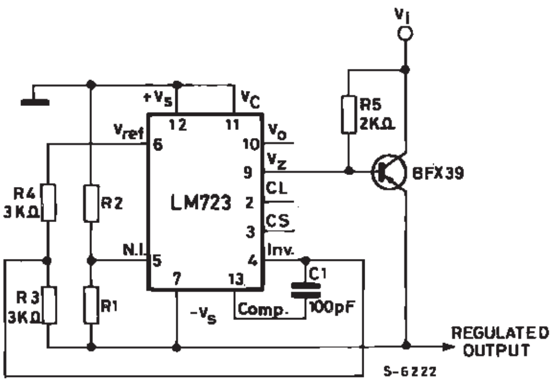
Note; $R_3 = \frac{R_1 \times R_2}{R_1 + R_2}$ for minimum temperature drift.
R3 may be eliminated for minimum component count.
Typical performance
Regulated Output Voltage........................ ....5V
Line Regulation (ΔV_i = 3V) 0.5mV
Load Regulation (ΔI_O = 50mA).................. .... 1.5mV

Figure 14 : Basic High Voltage Regulator (V_o = 7 to 37V).



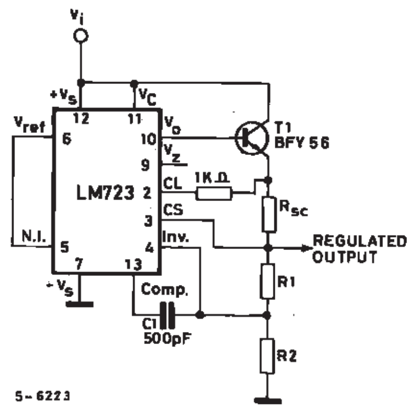
Note; $R_3 = \frac{R_1 \times R_2}{R_1 + R_2}$ for minimum temperature drift.
R3 may be eliminated for minimum component count.
Typical performance
Regulated Output Voltage........................ ....15V
Line Regulation (ΔV_i = 3V) 1.5mV
Load Regulation (ΔI_O = 50mA)................. .... 4.5mV

Figure 15 : Negative Voltage Regulator.



Typical performance
Regulated Output Voltage 15V
Line Regulation (ΔV_i = 3V)............ .... .1mV
Load Regulation (ΔI_O = 100mA) 2mV

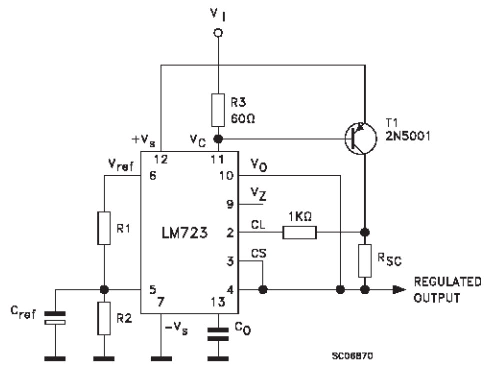
Figure 16 : Positive Voltage Regulator (external



Typical performance
Regulated Output Voltage............... .... + 15V
Line Regulation (ΔV_i = 3V) 1.5mV
Load Regulation (ΔI_O = 1A)............ .... 15mV

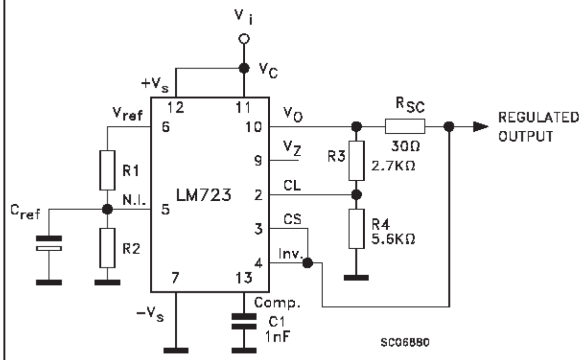
APPLICATION INFORMATION (continued).

Figure 17 : Positive Voltage Regulator (External PNP Pass Transistor)



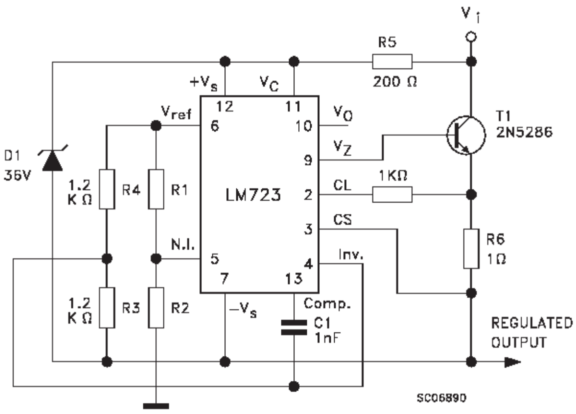
Typical performance
Regulated Output Voltage..5V
Line Regulation (ΔV_i = 3V)..0.5mV
Load Regulation (ΔI_O = 1 A)..1.5mV

Figure 18 : Foldback current limiting



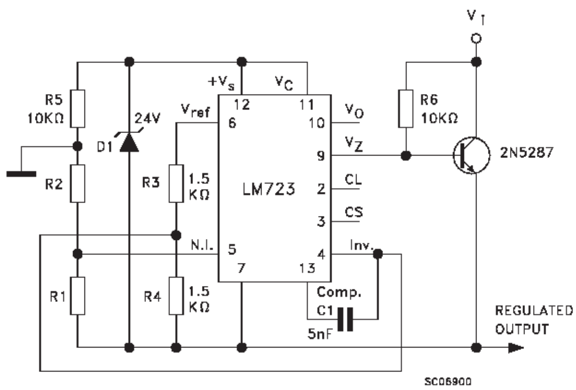
Typical performance
Regulated Output Voltage..5 V
Line Regulation (ΔV_i = 3V)..0.5mV
Load Regulation (ΔI_O = 10mA).......................................1mV
Current Limit Knee..20 mA

Figure 19 : Positive Floating Regulator



Typical performance
Regulated Output Voltage..100 V
Line Regulation (ΔV_i = 20V)..15 mV
Load Regulation (ΔI_O = 50mA)..20 mV

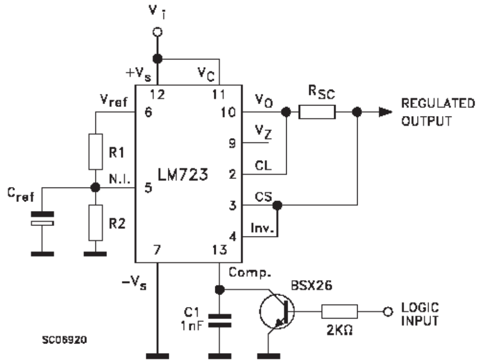
Figure 20 : Negative Floating Regulator



Typical performance
Regulated Output Voltage..- 100 V
Line Regulation (ΔV_i = 20V)..30 mV
Load Regulation (ΔI_O = 100 mA).......................................20 mV

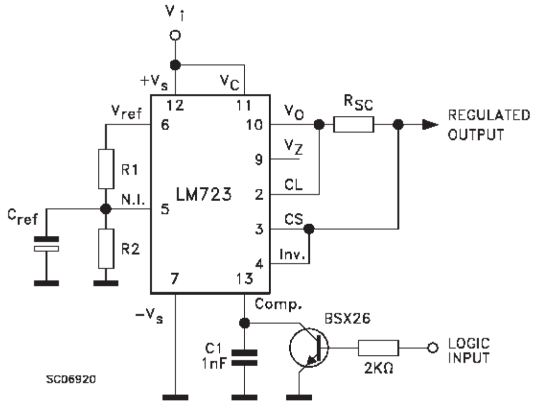
APPLICATION INFORMATION (continued).

Figure 21 : Positive Switching Regulator



Typical performance
Regulated Output Voltage...5 V
Line Regulation (ΔV_i = 30 V)..10 mV
Load Regulation (ΔI_O = 2 A)..80 mV

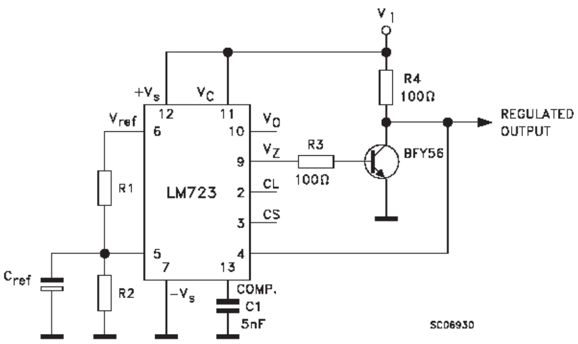
Figure 22 : Remote Shutdown Regulator With Current Limiting



Note: current limit transistor may be used for shutdown if current limiting is not required.

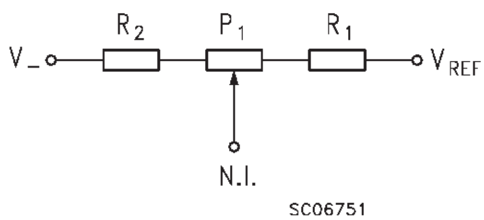
Typical performance
Regulated Output Voltage...5 V
Line Regulation (ΔV_i = 3 V)...0.5 mV
Load Regulation (ΔI_O = 50 mA)......................................1.5 mV

Figure 23 : Shunt Regulator.



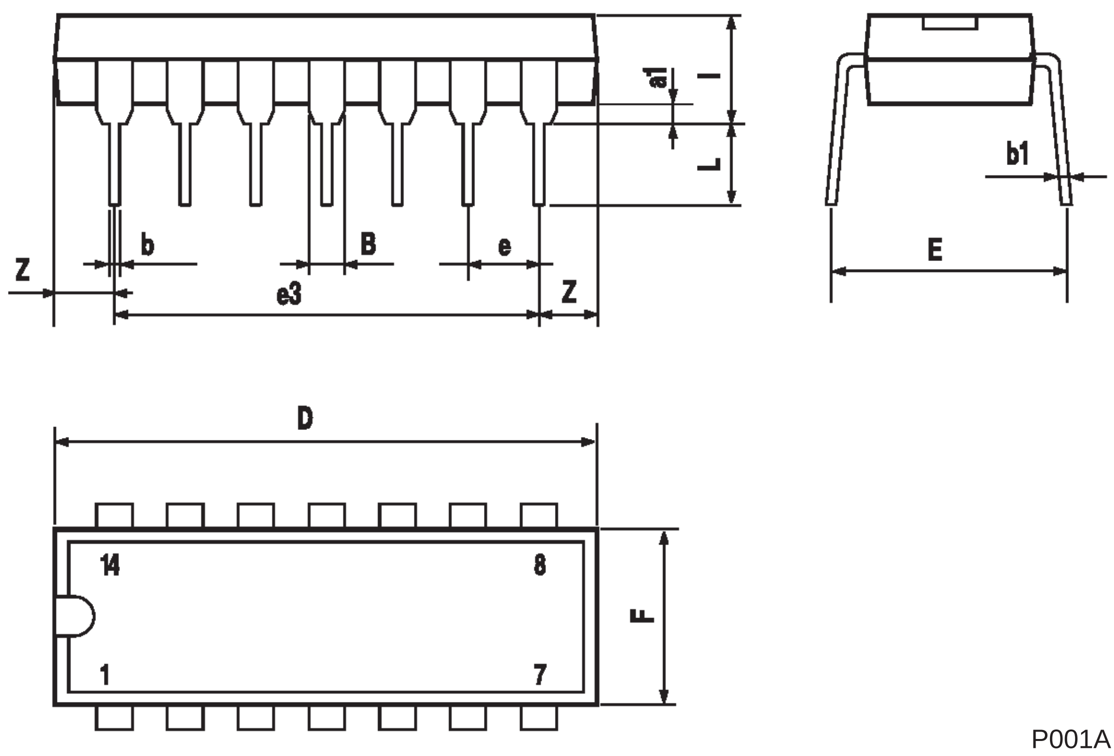
Typical performance
Regulated Output Voltage...5 V
Line Regulation (ΔV_i = 10 V)..2 mV
Load Regulation (ΔI_O = 100 mA)...5 mV

Figure 24 : Output Voltage Adjust



Plastic DIP-14 MECHANICAL DATA

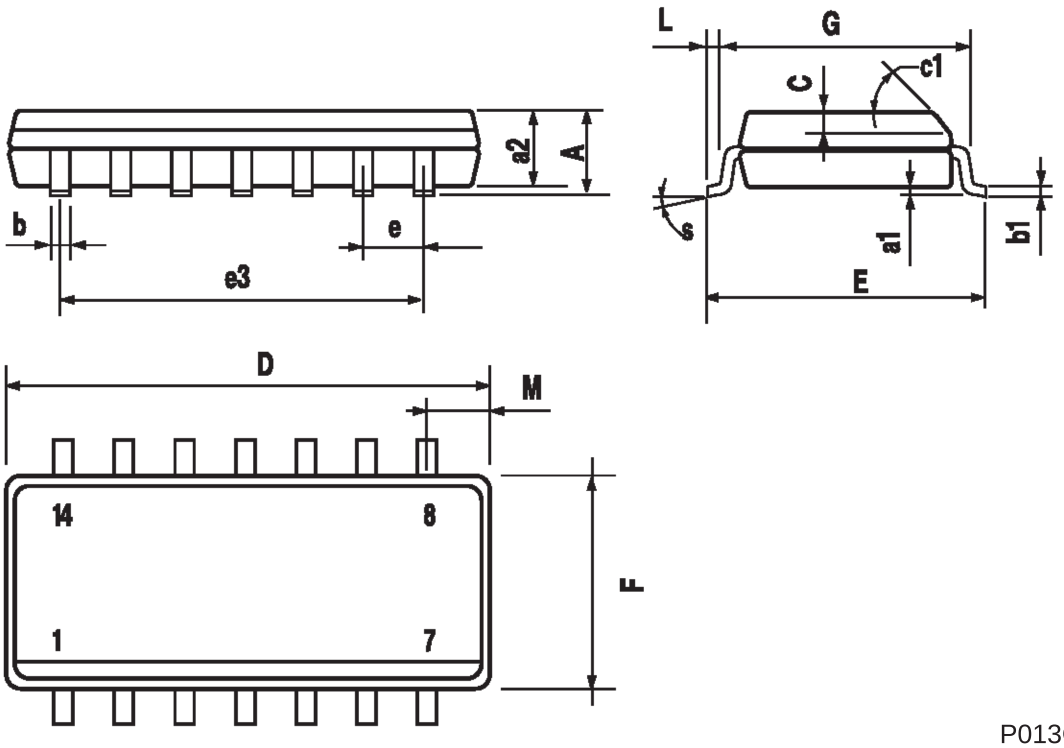
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



P001A

SO-14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8 (max.)					



P013G

.

National Semiconductor

January 2000

LM158/LM258/LM358/LM2904 Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

The LM358 is also available in a chip sized package (8-Bump micro SMD) using National's micro SMD package technology.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

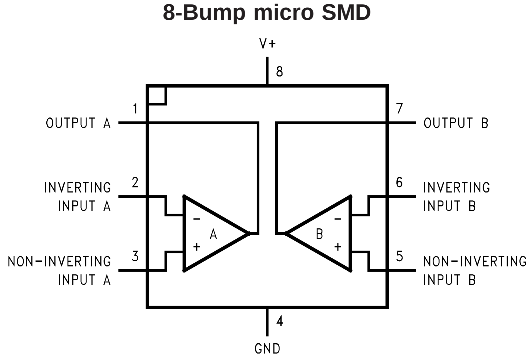
- Two internally compensated op amps
- Eliminates need for dual supplies
- Allows direct sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual op amp

Features

- Available in 8-Bump micro SMD chip sized package, (See AN-1112)
- Internally frequency compensated for unity gain
- Large dc voltage gain: 100 dB
- Wide bandwidth (unity gain): 1 MHz (temperature compensated)
- Wide power supply range:
  — Single supply: 3V to 32V
  — or dual supplies: ±1.5V to ±16V
- Very low supply current drain (500 µA) — essentially independent of supply voltage
- Low input offset voltage: 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing: 0V to V^{+}− 1.5V

Connection Diagrams

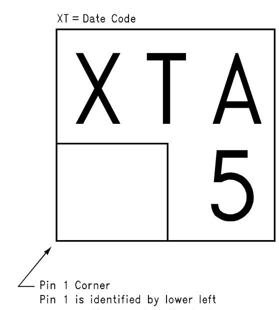
8-Bump micro SMD



DS007787-55

Top View (Bump Side Down)

micro SMD Marking Orientation



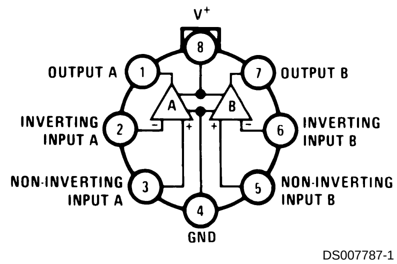
DS007787-56

Bumps are numbered counter-clockwise.

Top View

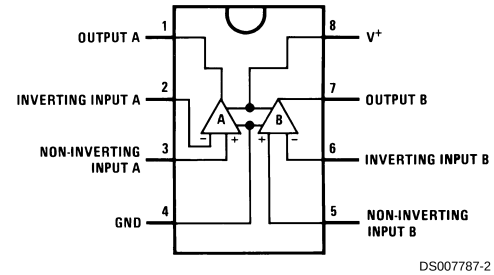
Connection Diagrams (Continued)

Metal Can Package



Top View

DIP/SO Package



Top View

Ordering Information

Package	Temperature Range				NSC Drawing
	−55˚C to 125˚C	−25˚C to 85˚C	0˚C to 70˚C	−40˚C to 85˚C	
SO-8			LM358AM LM358M	LM2904M	M08A
8-Pin Molded DIP			LM358AN LM358N	LM2904N	N08E
8-Pin Ceramic DIP	LM158AJ/883(Note 1) LM158J/883(Note 1) LM158J LM158AJLQML(Note 2) LM158AJQMLV(Note 2)				J08A
TO-5, 8-Pin Metal Can	LM158AH/883(Note 1) LM158H/883(Note 1) LM158AH LM158H LM158AHLQML(Note 2) LM158AHLQMLV(Note 2)	LM258H	LM358H		H08C
8-Bump micro SMD			LM358BP LM358BPX		BPA08AAA

Note 1: LM158 is available per SMD #5962-8771001

LM158A is available per SMD #5962-8771002

Note 2: See STD Mil DWG 5962L87710 for Radiation Tolerant Devices

Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Supply Voltage, V^+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Power Dissipation (Note 3)		
Molded DIP	830 mW	830 mW
Metal Can	550 mW	
Small Outline Package (M)	530 mW	530 mW
micro SMD	435mW	
Output Short-Circuit to GND		
(One Amplifier) (Note 4)		
$V^+ \leq 15V$ and $T_A = 25˚C$	Continuous	Continuous
Input Current ($V_{IN} < −0.3V$) (Note 5)	50 mA	50 mA
Operating Temperature Range		
LM358	0˚C to +70˚C	−40˚C to +85˚C
LM258	−25˚C to +85˚C	
LM158	−55˚C to +125˚C	
Storage Temperature Range	−65˚C to +150˚C	−65˚C to +150˚C
Lead Temperature, DIP		
(Soldering, 10 seconds)	260˚C	260˚C
Lead Temperature, Metal Can		
(Soldering, 10 seconds)	300˚C	300˚C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260˚C	260˚C
Small Outline Package		
Vapor Phase (60 seconds)	215˚C	215˚C
Infrared (15 seconds)	220˚C	220˚C

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

ESD Tolerance (Note 12)	250V	250V

Electrical Characteristics

$V^+ = +5.0V$, unless otherwise stated

Parameter	Conditions	LM158A			LM358A			LM158/LM258			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 7), $T_A = 25˚C$		1	2		2	3		2	5	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(−)}$, $T_A = 25˚C$, $V_{CM} = 0V$, (Note 8)		20	50		45	100		45	150	nA
Input Offset Current	$I_{IN(+)} − I_{IN(−)}$, $V_{CM} = 0V$, $T_A = 25˚C$		2	10		5	30		3	30	nA
Input Common-Mode Voltage Range	$V^+ = 30V$, (Note 9) (LM2904, $V^+ = 26V$), $T_A = 25˚C$	0		$V^+−1.5$	0		$V^+−1.5$	0		$V^+−1.5$	V
Supply Current	Over Full Temperature Range $R_L = \infty$ on All Op Amps										
	$V^+ = 30V$ (LM2904 $V^+ = 26V$)		1	2		1	2		1	2	mA
	$V^+ = 5V$		0.5	1.2		0.5	1.2		0.5	1.2	mA

Electrical Characteristics

$V^+ = +5.0V$, unless otherwise stated

Parameter	Conditions	LM358			LM2904			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 7) , $T_A = 25^{\circ}C$		2	7		2	7	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25^{\circ}C$, $V_{CM} = 0V$, (Note 8)		45	250		45	250	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25^{\circ}C$		5	50		5	50	nA
Input Common-Mode Voltage Range	$V^+ = 30V$, (Note 9) (LM2904, $V^+ = 26V$), $T_A = 25^{\circ}C$	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	Over Full Temperature Range $R_L = \infty$ on All Op Amps							
	$V^+ = 30V$ (LM2904 $V^+ = 26V$)		1	2		1	2	mA
	$V^+ = 5V$		0.5	1.2		0.5	1.2	mA

Electrical Characteristics

$V^+ = +5.0V$, (Note 6), unless otherwise stated

Parameter		Conditions	LM158A			LM358A			LM158/LM258			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		$V^+ = 15V$, $T_A = 25^{\circ}C$, $R_L \geq 2\ k\Omega$, (For $V_O = 1V$ to 11V)	50	100		25	100		50	100		V/mV
Common-Mode Rejection Ratio		$T_A = 25^{\circ}C$, $V_{CM} = 0V$ to $V^+-1.5V$	70	85		65	85		70	85		dB
Power Supply Rejection Ratio		$V^+ = 5V$ to 30V (LM2904, $V^+ = 5V$ to 26V), $T_A = 25^{\circ}C$	65	100		65	100		65	100		dB
Amplifier-to-Amplifier Coupling		f = 1 kHz to 20 kHz, $T_A = 25^{\circ}C$ (Input Referred), (Note 10)		−120			−120			−120		dB
Output Current	Source	$V_{IN}^+ = 1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25^{\circ}C$	20	40		20	40		20	40		mA
	Sink	$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$ $V^+ = 15V$, $T_A = 25^{\circ}C$, $V_O = 2V$	10	20		10	20		10	20		mA
		$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$ $T_A = 25^{\circ}C$, $V_O = 200$ mV, $V^+ = 15V$	12	50		12	50		12	50		µA
Short Circuit to Ground		$T_A = 25^{\circ}C$, (Note 4), $V^+ = 15V$		40	60		40	60		40	60	mA
Input Offset Voltage		(Note 7)			4			5			7	mV
Input Offset Voltage Drift		$R_S = 0\Omega$		7	15		7	20		7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			30			75			100	nA
Input Offset Current Drift		$R_S = 0\Omega$		10	200		10	300		10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	200		40	300	nA
Input Common-Mode Voltage Range		$V^+ = 30$ V, (Note 9) (LM2904, $V^+ = 26V$)	0		V^+-2	0		V^+-2	0		V^+-2	V

Electrical Characteristics (Continued)

$V^+ = +5.0V$, (Note 6), unless otherwise stated

Parameter		Conditions		LM158A			LM358A			LM158/LM258			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		$V^+ = +15V$ (V_O = 1V to 11V) $R_L \geq 2$ kΩ		25			15			25			V/mV
Output Voltage Swing	V_{OH}	$V^+ = +30V$ (LM2904, $V^+ = 26V$)	R_L = 2 kΩ	26			26			26			V
			R_L = 10 kΩ	27	28		27	28		27	28		V
	V_{OL}	$V^+ = 5V$, R_L = 10 kΩ			5	20		5	20		5	20	mV
Output Current	Source	$V_{IN}^+ = +1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$		10	20		10	20		10	20		mA
	Sink	$V_{IN}^- = +1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $V_O = 2V$		10	15		5	8		5	8		mA

Electrical Characteristics

$V^+ = +5.0V$, (Note 6), unless otherwise stated

Parameter		Conditions	LM358			LM2904			Units
			Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		$V^+ = 15V$, $T_A = 25°C$, $R_L \geq 2$ kΩ, (For V_O = 1V to 11V)	25	100		25	100		V/mV
Common-Mode Rejection Ratio		$T_A = 25°C$, V_{CM} = 0V to $V^+-1.5V$	65	85		50	70		dB
Power Supply Rejection Ratio		V^+ = 5V to 30V (LM2904, V^+ = 5V to 26V), $T_A = 25°C$	65	100		50	100		dB
Amplifier-to-Amplifier Coupling		f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred), (Note 10)		−120			−120		dB
Output Current	Source	$V_{IN}^+ = 1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25°C$	20	40		20	40		mA
	Sink	$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$ $V^+ = 15V$, $T_A = 25°C$, $V_O = 2V$	10	20		10	20		mA
		$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$ $T_A = 25°C$, V_O = 200 mV, $V^+ = 15V$	12	50		12	50		µA
Short Circuit to Ground		$T_A = 25°C$, (Note 4), $V^+ = 15V$		40	60		40	60	mA
Input Offset Voltage		(Note 7)			9			10	mV
Input Offset Voltage Drift		$R_S = 0Ω$		7			7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			150		45	200	nA
Input Offset Current Drift		$R_S = 0Ω$		10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	500		40	500	nA
Input Common-Mode Voltage Range		V^+ = 30 V, (Note 9) (LM2904, $V^+ = 26V$)	0		V^+-2	0		V^+-2	V

Electrical Characteristics (Continued)

$V^+ = +5.0V$, (Note 6), unless otherwise stated

Parameter		Conditions		LM358			LM2904			Units
				Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		$V^+ = +15V$ (V_O = 1V to 11V) $R_L \geq 2\ k\Omega$		15			15			V/mV
Output Voltage Swing	V_{OH}	$V^+ = +30V$ (LM2904, $V^+ = 26V$)	$R_L = 2\ k\Omega$	26			22			V
			$R_L = 10\ k\Omega$	27	28		23	24		V
	V_{OL}	$V^+ = 5V$, $R_L = 10\ k\Omega$			5	20		5	100	mV
Output Current	Source	$V_{IN}^+ = +1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$		10	20		10	20		mA
	Sink	$V_{IN}^- = +1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $V_O = 2V$		5	8		5	8		mA

Note 3: For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a +125˚C maximum junction temperature and a thermal resistance of 120˚C/W for MDIP, 182˚C/W for Metal Can, 189˚C/W for Small Outline package, and 230˚C/W for micro SMD, which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a +150˚C maximum junction temperature. The dissipation is the total of both amplifiers — use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 4: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short cirucits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 5: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25˚C).

Note 6: These specifications are limited to $-55˚C \leq T_A \leq +125˚C$ for the LM158/LM158A. With the LM258/LM258A, all temperature specifications are limited to $-25˚C \leq T_A \leq +85˚C$, the LM358/LM358A temperature specifications are limited to $0˚C \leq T_A \leq +70˚C$, and the LM2904 specifications are limited to $-40˚C \leq T_A \leq +85˚C$.

Note 7: $V_O \cong 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+ −1.5V) at 25˚C. For LM2904, V^+ from 5V to 26V.

Note 8: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 9: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25˚C). The upper end of the common-mode voltage range is V^+ −1.5V (at 25˚C), but either or both inputs can go to +32V without damage (+26V for LM2904), independent of the magnitude of V^+.

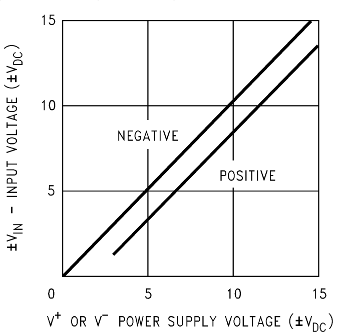
Note 10: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 11: Refer to RETS158AX for LM158A military specifications and to RETS158X for LM158 military specifications.

Note 12: Human body model, 1.5 kΩ in series with 100 pF.

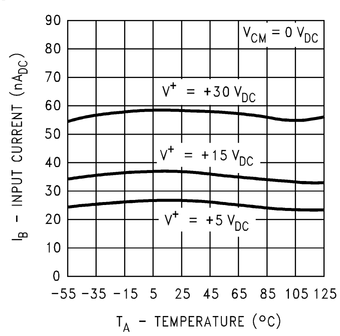
Typical Performance Characteristics

Input Voltage Range



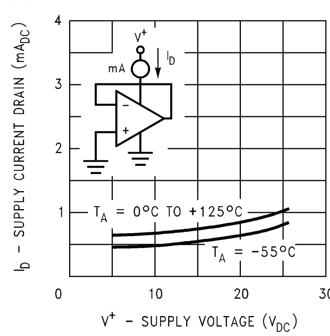
DS007787-34

Input Current



DS007787-35

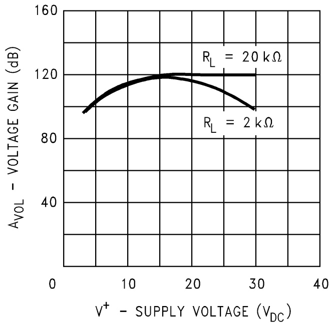
Supply Current



DS007787-36

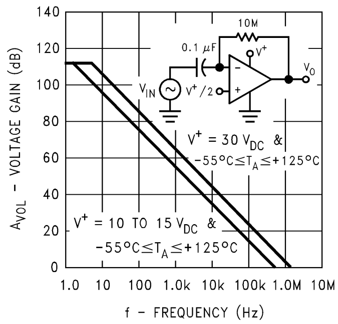
Typical Performance Characteristics (Continued)

Voltage Gain



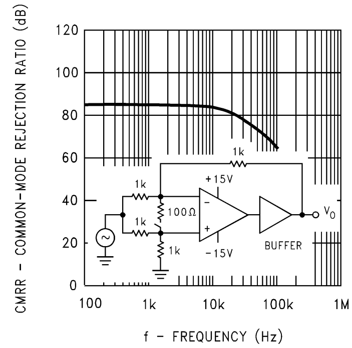
DS007787-37

Open Loop Frequency Response



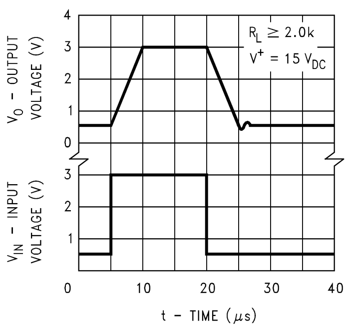
DS007787-38

Common-Mode Rejection Ratio



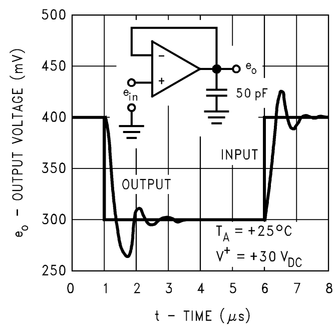
DS007787-39

Voltage Follower Pulse Response



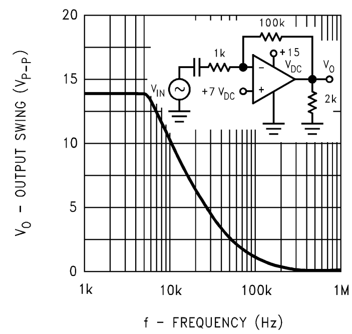
DS007787-40

Voltage Follower Pulse Response (Small Signal)



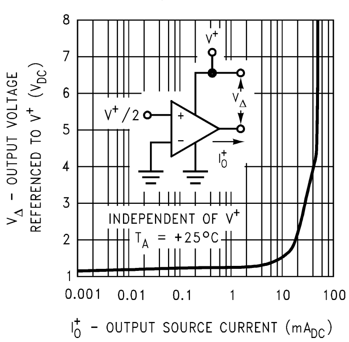
DS007787-41

Large Signal Frequency Response



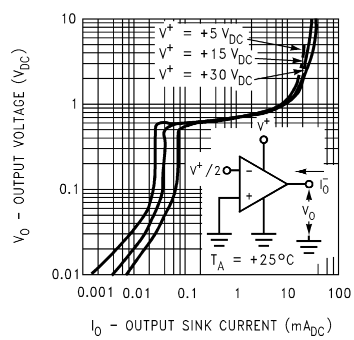
DS007787-42

Output Characteristics Current Sourcing



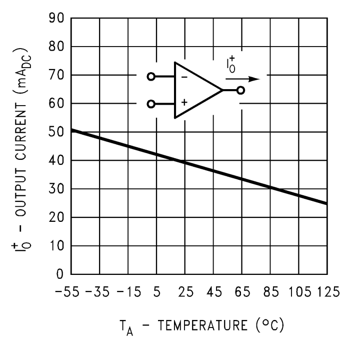
DS007787-43

Output Characteristics Current Sinking



DS007787-44

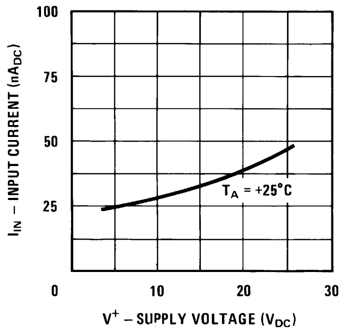
Current Limiting



DS007787-45

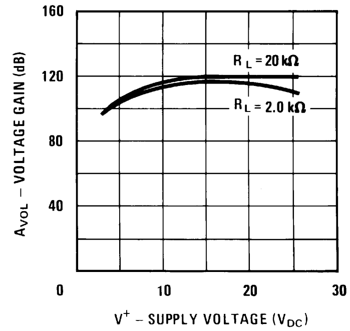
Typical Performance Characteristics (Continued)

Input Current (LM2902 only)



DS007787-46

Voltage Gain (LM2902 only)



DS007787-47

Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25˚C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accomodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25˚C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accomodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

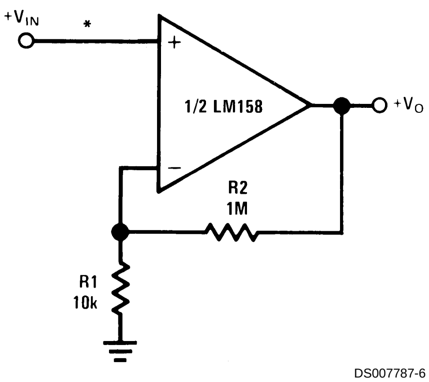
The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 3 V_{DC} to 30 V_{DC}.

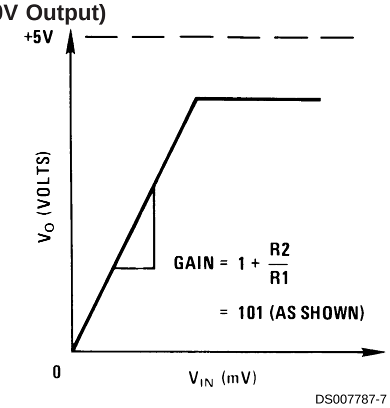
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive function temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25˚C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$)

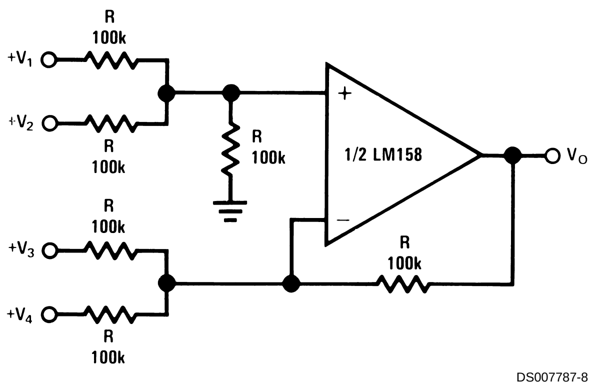
Non-Inverting DC Gain (0V Output)





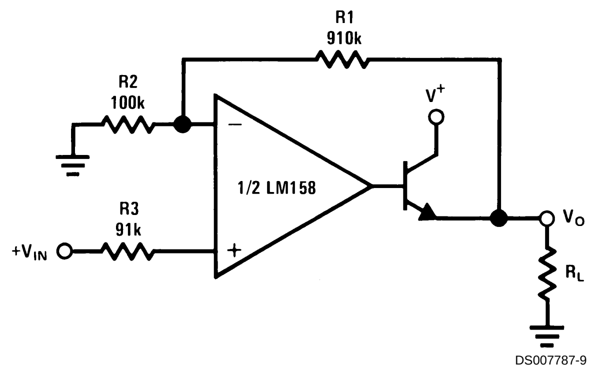
*R not needed due to temperature independent I_{IN}

DC Summing Amplifier ($V_{IN'S} \geq 0\ V_{DC}$ and $V_O \geq 0\ V_{DC}$)



Where: $V_O = V_1 + V_2 + V_3 + V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

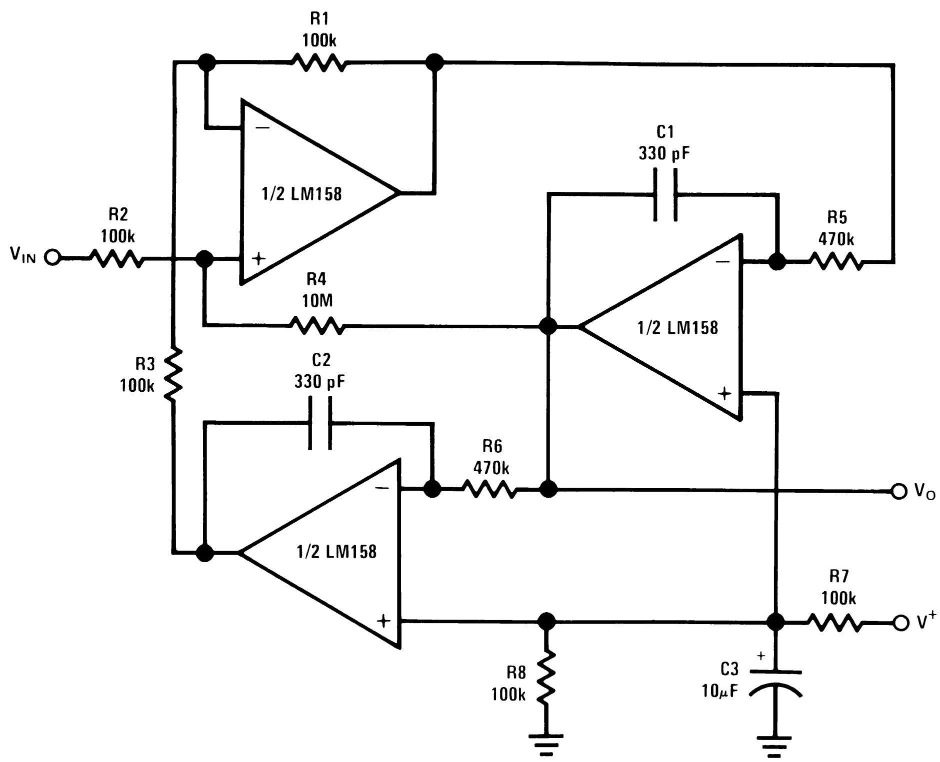
Power Amplifier



$V_O = 0\ V_{DC}$ for $V_{IN} = 0\ V_{DC}$
$A_V = 10$

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

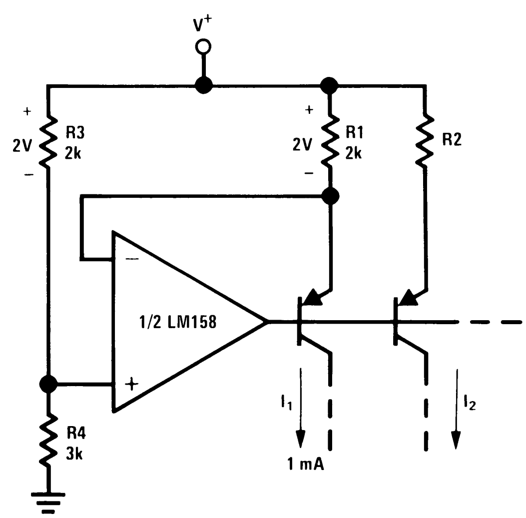
"BI-QUAD" RC Active Bandpass Filter



DS007787-10

f_O = 1 kHz
Q = 50
A_V = 100 (40 dB)

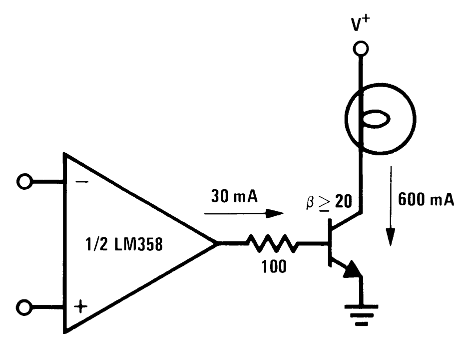
Fixed Current Sources



DS007787-11

$$I_2 = \left(\frac{R1}{R2}\right) I_1$$

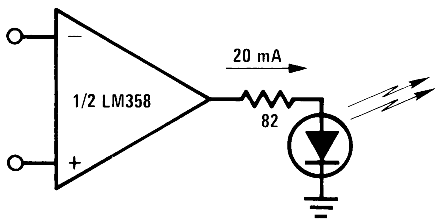
Lamp Driver



DS007787-12

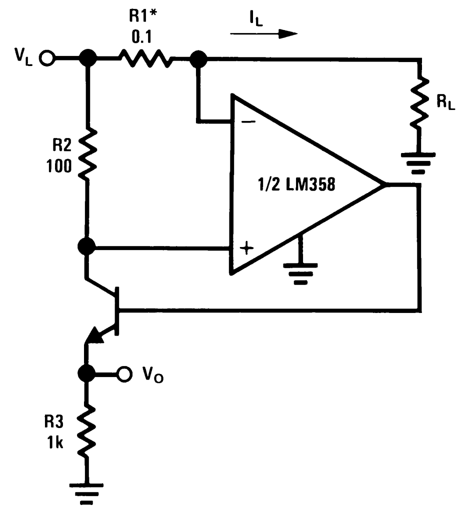
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

LED Driver



DS007787-13

Current Monitor

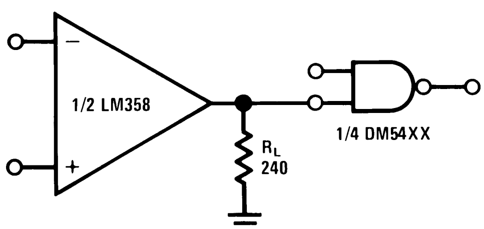


DS007787-14

$$V_O = \frac{1V\ (I_L)}{1A}$$

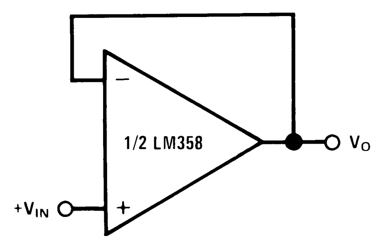
*(Increase R1 for I_L small)
$V_L \leq V^+ - 2V$

Driving TTL



DS007787-15

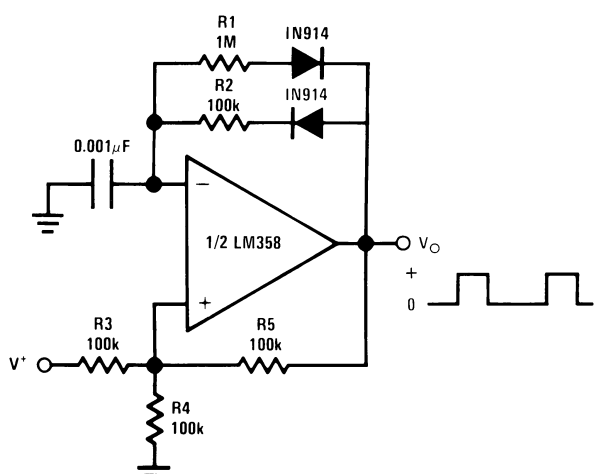
Voltage Follower



DS007787-17

$V_O = V_{IN}$

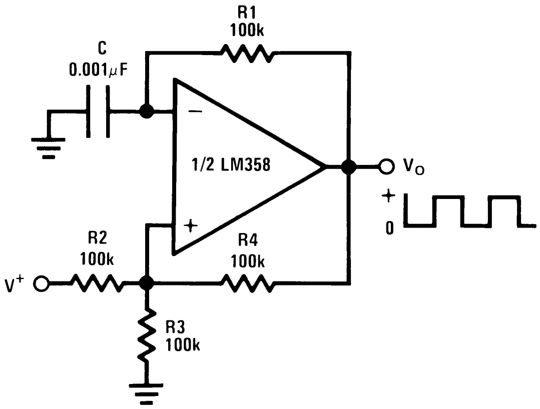
Pulse Generator



DS007787-16

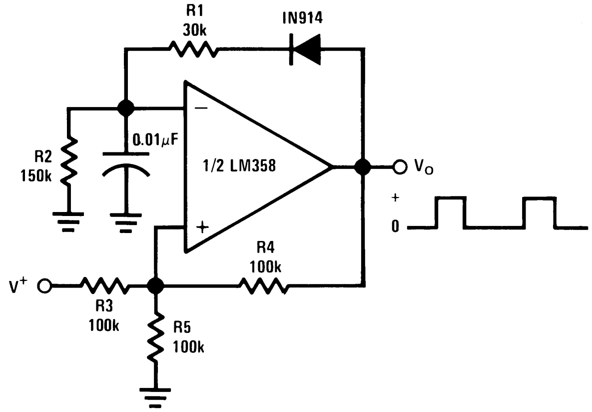
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Squarewave Oscillator



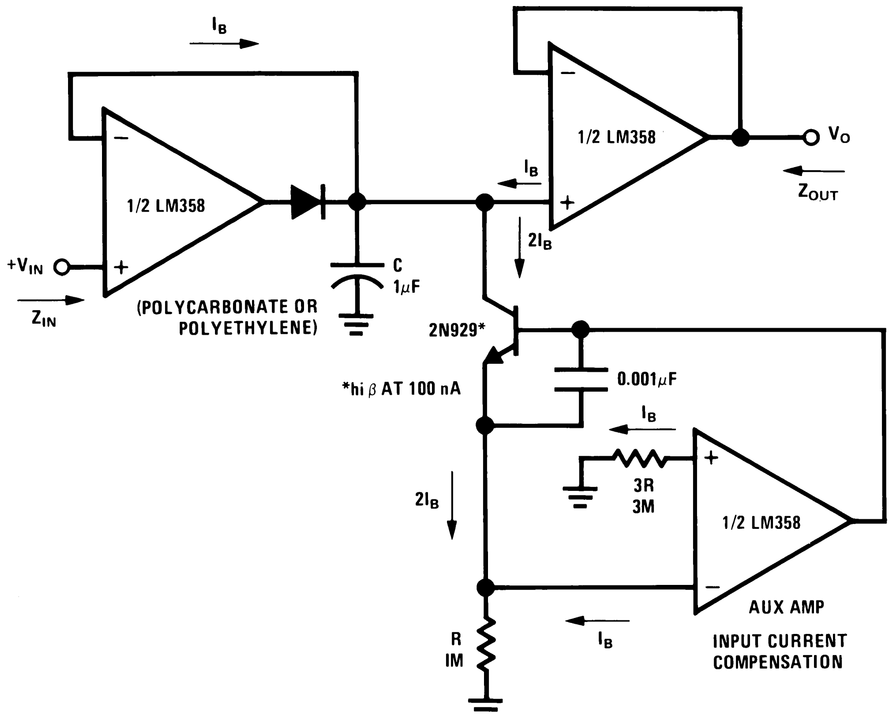
DS007787-18

Pulse Generator



DS007787-19

Low Drift Peak Detector

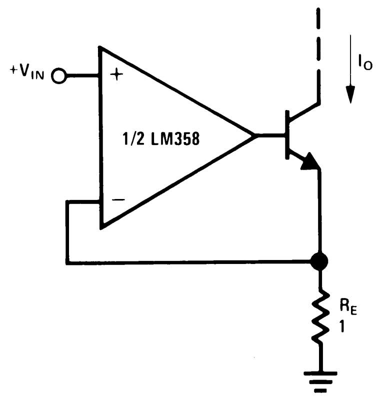


DS007787-20

HIGH Z_{IN}
LOW Z_{OUT}

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

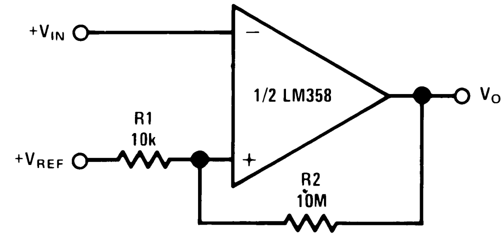
High Compliance Current Sink



DS007787-21

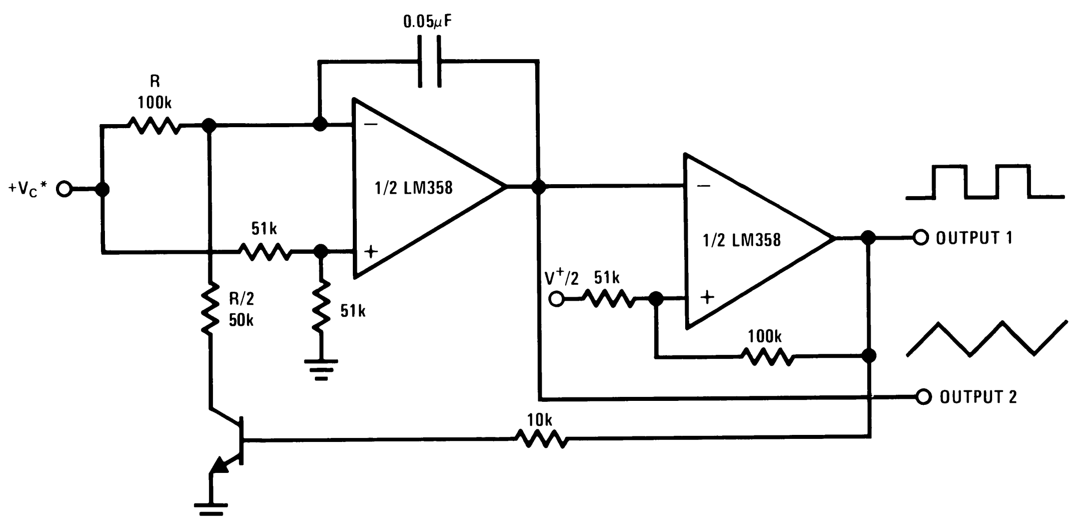
I_O = 1 amp/volt V_{IN}
(Increase R_E for I_O small)

Comparator with Hysteresis



DS007787-22

Voltage Controlled Oscillator (VCO)

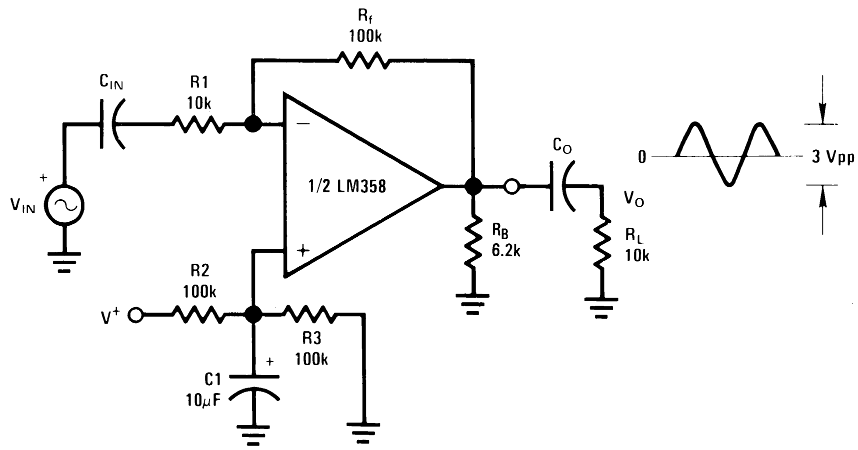


DS007787-23

*WIDE CONTROL VOLTAGE RANGE: 0 $V_{DC} \le V_C \le 2\ (V^+ - 1.5V_{DC})$

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

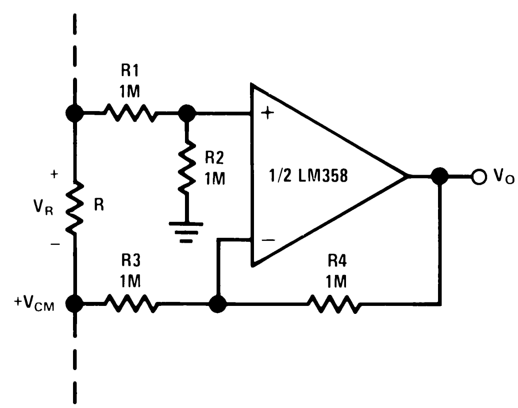
AC Coupled Inverting Amplifier



DS007787-24

$$A_V = \frac{R_f}{R1} \text{ (As shown, } A_V = 10)$$

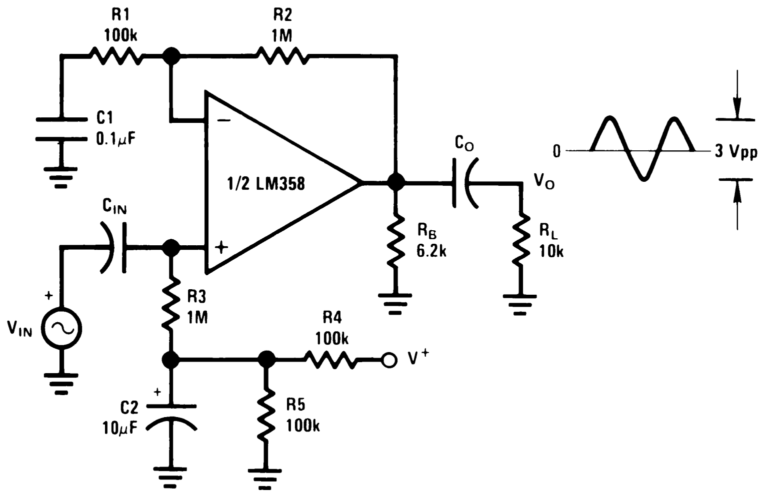
Ground Referencing a Differential Input Signal



DS007787-25

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

AC Coupled Non-Inverting Amplifier

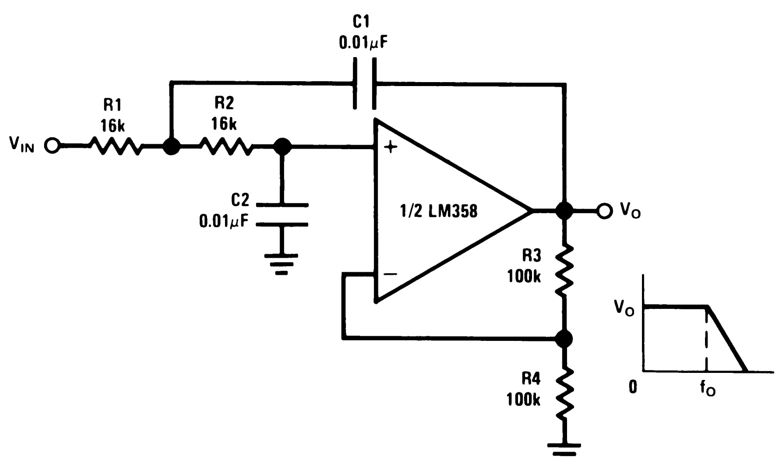


DS007787-26

$$A_V = 1 + \frac{R2}{R1}$$

A_V = 11 (As Shown)

DC Coupled Low-Pass RC Active Filter

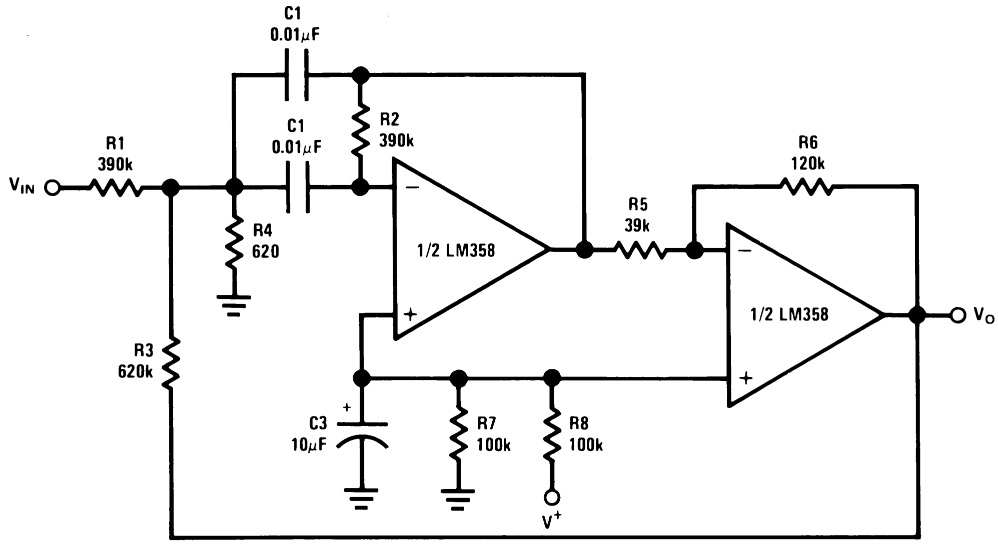


DS007787-27

f_o = 1 kHz
Q = 1
A_V = 2

Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

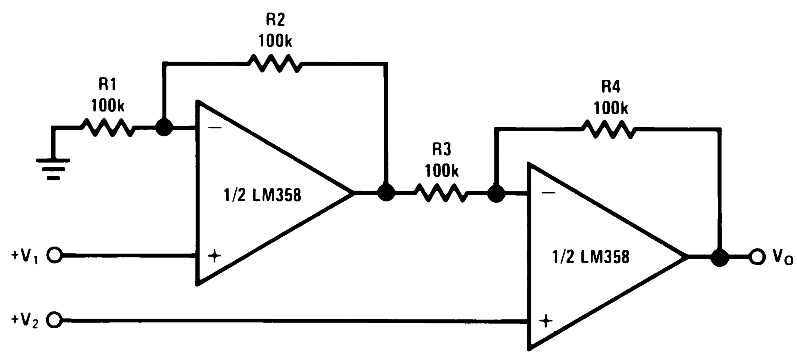
Bandpass Active Filter



DS007787-28

$f_o = 1$ kHz
Q = 25

High Input Z, DC Differential Amplifier



DS007787-29

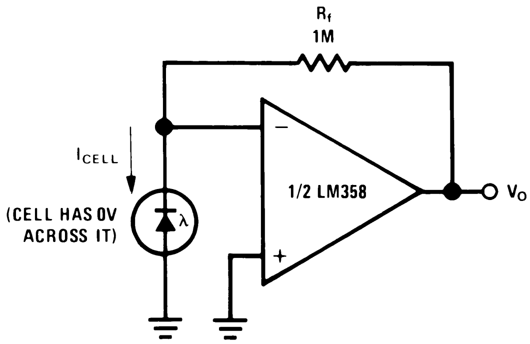
For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3} (V_2 - V_1)$

As Shown: $V_O = 2 (V_2 - V_1)$

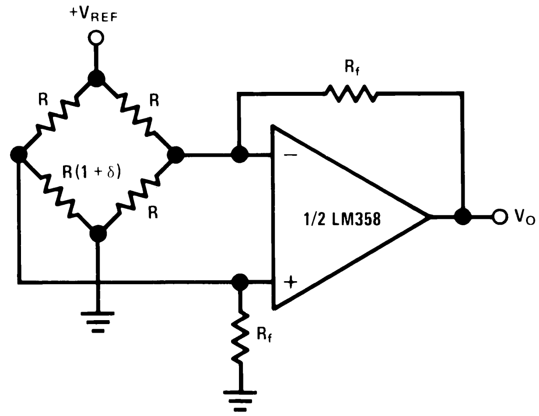
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Photo Voltaic-Cell Amplifier



DS007787-30

Bridge Current Amplifier

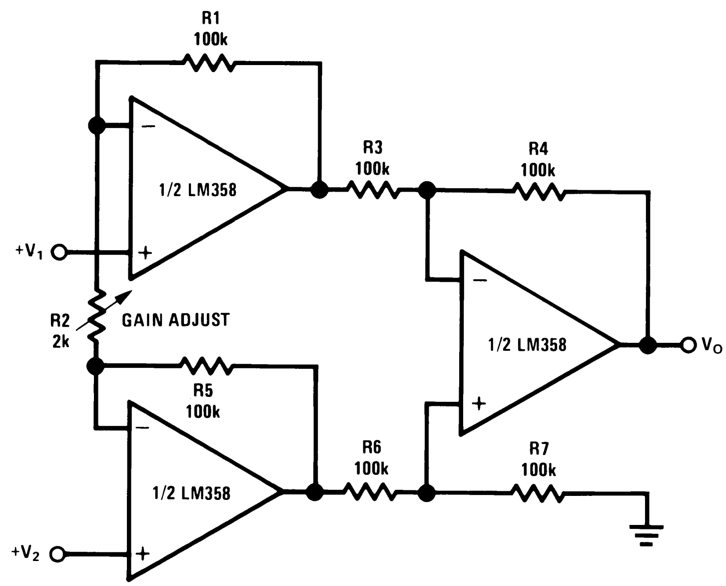


DS007787-33

For $\delta << 1$ and $R_f >> R$

$$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

High Input Z Adjustable-Gain DC Instrumentation Amplifier



DS007787-31

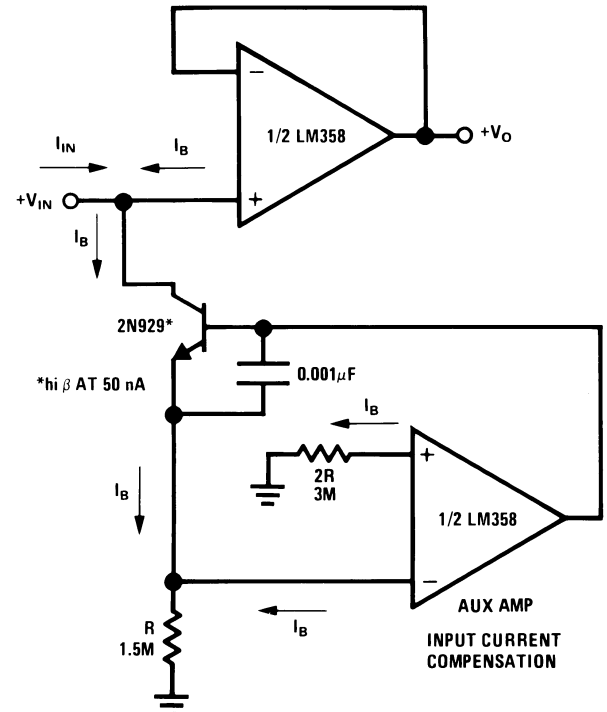
If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2}\ (V_2 - V_1)$$

As shown $V_O = 101\ (V_2 - V_1)$

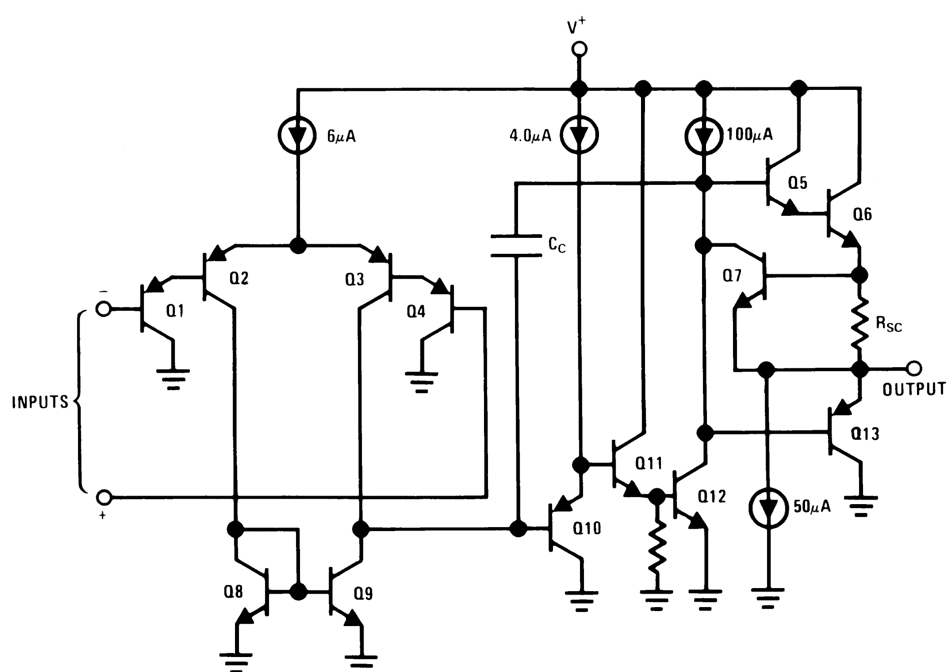
Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



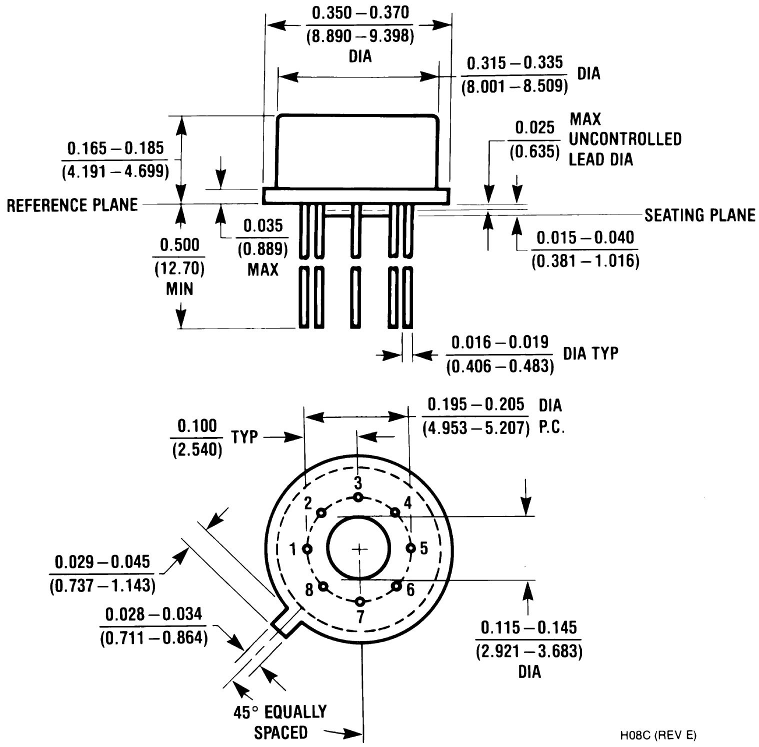
DS007787-32

Schematic Diagram (Each Amplifier)

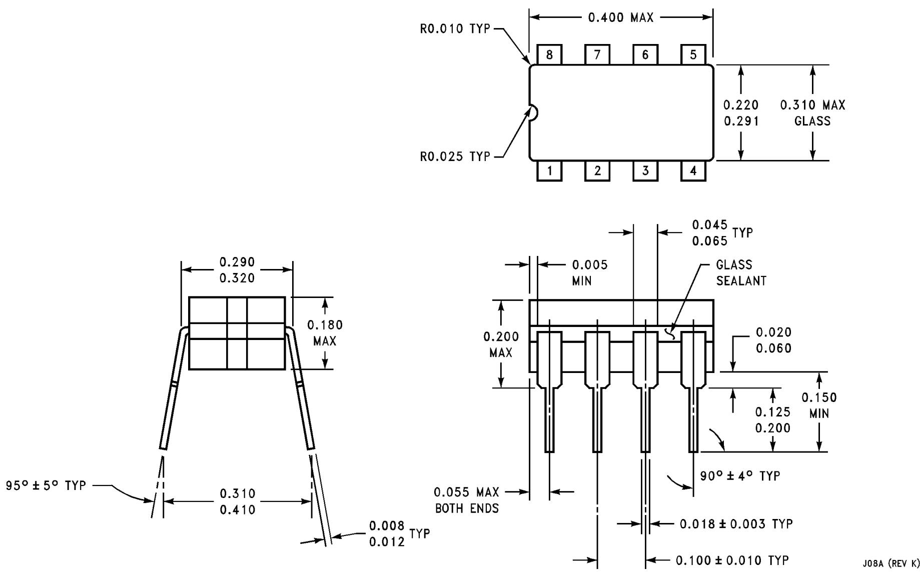


DS007787-3

Physical Dimensions inches (millimeters) unless otherwise noted

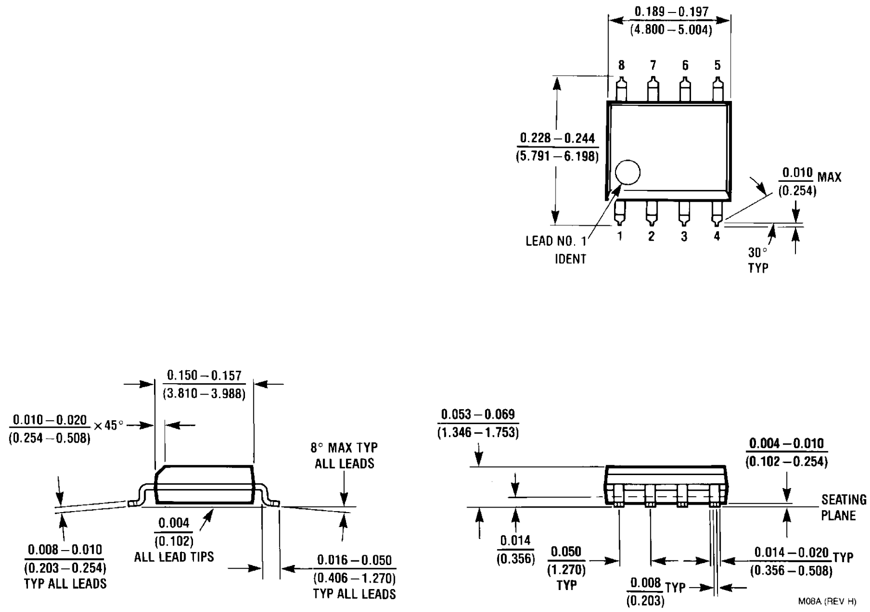


Metal Can Package (H)
Order Number LM158AH, LM158AH/883, LM158H,
LM158H/883, LM258H or LM358H
NS Package Number H08C



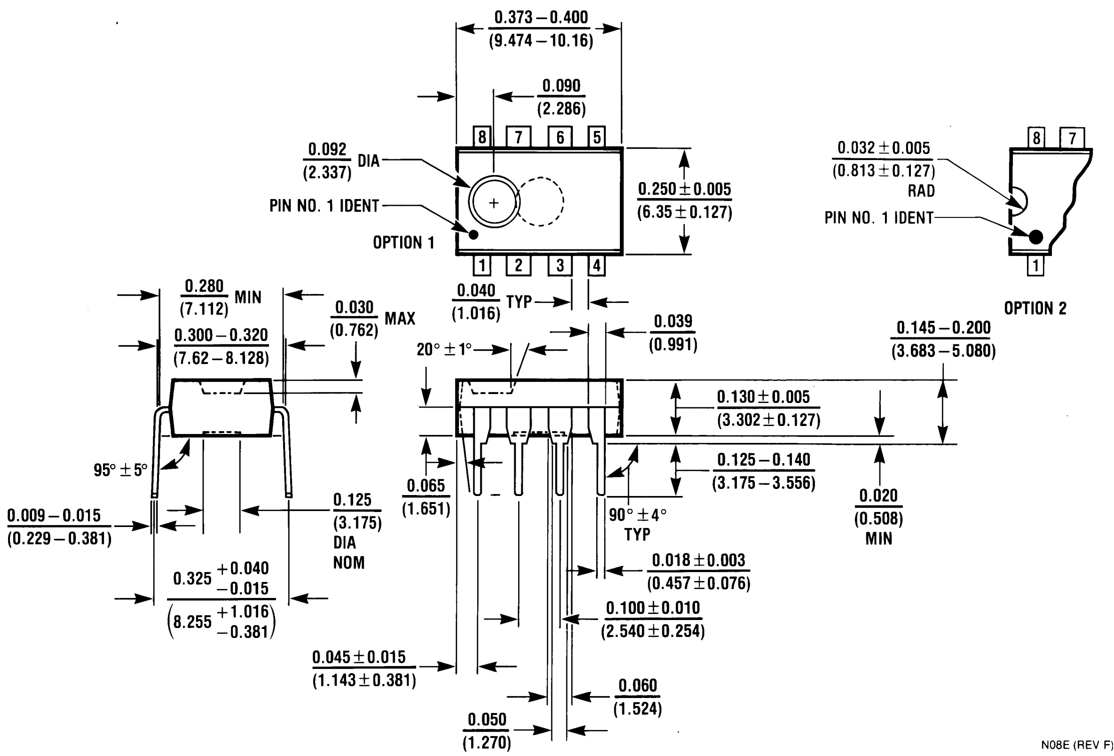
Cerdip Package (J)
Order Number LM158J, LM158J/883, LM158AJ or LM158AJ/883
NS Package Number J08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



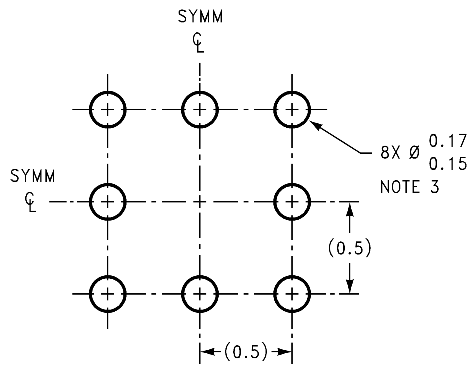
S.O. Package (M)
Order Number LM358M, LM358AM or LM2904M
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

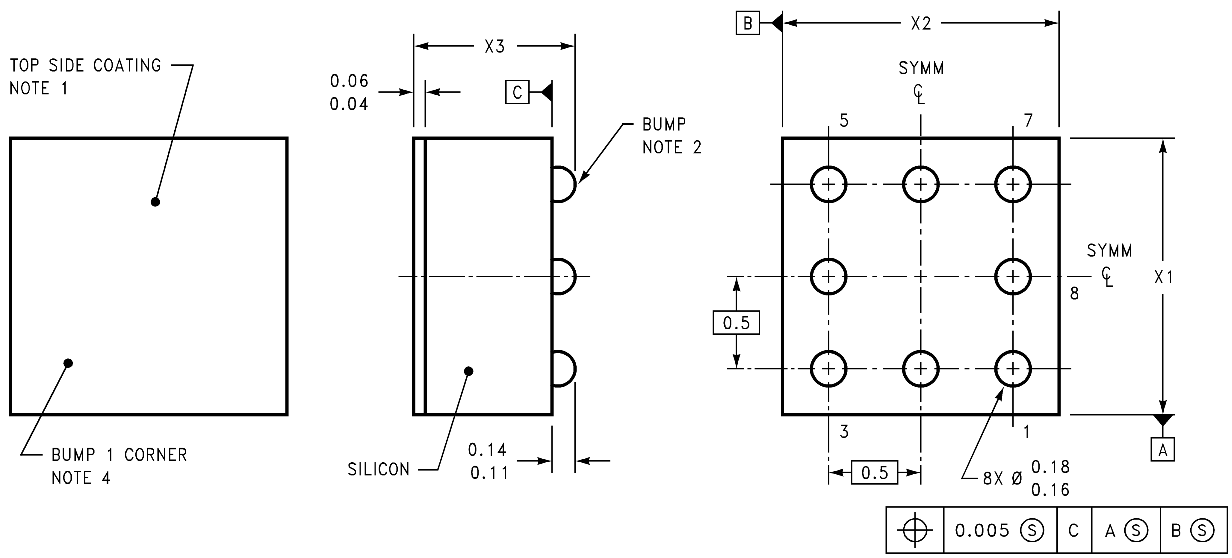


Molded Dip Package (N)
Order Number LM358AN, LM358N or LM2904N
NS Package Number N08E

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

BPA08XXX (REV A)

NOTES: UNLESS OTHERWISE SPECIFIED

1. EPOXY COATING
2. 63Sn/37Pb EUTECTIC BUMP
3. RECOMMEND NON-SOLDER MASK DEFINED LANDING PAD.
4. PIN 1 IS ESTABLISHED BY LOWER LEFT CORNER WITH RESPECT TO TEXT ORIENTATION REMAINING PINS ARE NUMBERED COUNTERCLOCKWISE.
5. XXX IN DRAWING NUMBER REPRESENTS PACKAGE SIZE VARIATION WHERE X_1 IS PACKAGE WIDTH, X_2 IS PACKAGE LENGTH AND X_3 IS PACKAGE HEIGHT.
6. REFERENCE JEDEC REGISTRATION MO-211, VARIATION BC.

8-Bump micro SMD
NS Package Number BPA08AAA
X_1 = 1.285 X_2 = 1.285 X_3 = 0.700

Notes

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507

MC14511B

BCD-To-Seven Segment Latch/Decoder/Driver

The MC14511B BCD–to–seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4–bit storage latch, an 8421 BCD–to–seven segment decoder, and an output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn–off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven–segment light–emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

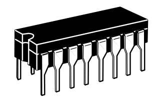
Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High–Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low–power TTL Loads, One Low–power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Chip Complexity: 216 FETs or 54 Equivalent Gates
- Triple Diode Protection on all Inputs

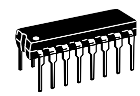
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 18	V
Input Voltage, All Inputs	V_{in}	– 0.5 to V_{DD} +0.5	V
DC Current Drain per Input Pin	I	10	mA
Operating Temperature Range	T_A	– 55 to + 125	°C
Power Dissipation per Package†	P_D	500	mW
Storage Temperature Range	T_{stg}	– 65 to + 150	°C
Maximum Output Drive Current (Source) per Output	I_{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output ‡	P_{OHmax}	50	mW

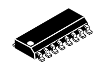
‡$P_{OHmax} = I_{OH} (V_{DD} – V_{OH})$
* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C



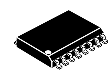
L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B



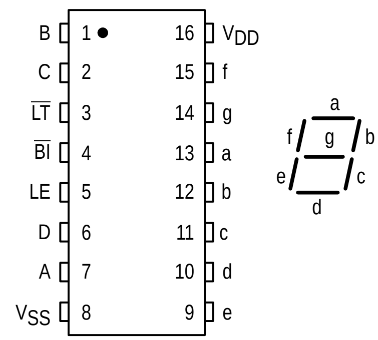
DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

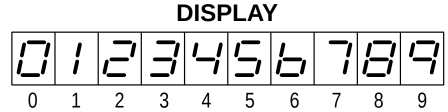
MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBDW	SOIC
MC14XXXBD	SOIC

T_A = – 55° to 125°C for all packages.

PIN ASSIGNMENT



DISPLAY



TRUTH TABLE

Inputs							Outputs							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	1	1	1	1	1	0	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X				*				*

X = Don't Care
* Depends upon the BCD code previously applied when LE = 0

REV 3
1/94

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic		Symbol	V_{DD} Vdc	– 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ #	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ or 0	"0" Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
			10	—	0.05	—	0	0.05	—	0.05	
			15	—	0.05	—	0	0.05	—	0.05	
$V_{in} = 0$ or V_{DD}	"1" Level	V_{OH}	5.0	4.1	—	4.1	4.57	—	4.1	—	Vdc
			10	9.1	—	9.1	9.58	—	9.1	—	
			15	14.1	—	14.1	14.59	—	14.1	—	
Input Voltage #	"0" Level	V_{IL}									Vdc
(V_O = 3.8 or 0.5 Vdc)			5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 8.8 or 1.0 Vdc)			10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.8 or 1.5 Vdc)			15	—	4.0	—	6.75	4.0	—	4.0	
	"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 3.8 Vdc)			5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 8.8 Vdc)			10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.8 Vdc)			15	11	—	11	8.25	—	11	—	
Output Drive Voltage		V_{OH}									Vdc
(I_{OH} = 0 mA)	Source		5.0	4.1	—	4.1	4.57	—	4.1	—	
(I_{OH} = 5.0 mA)				—	—	—	4.24	—	—	—	
(I_{OH} = 10 mA)				3.9	—	3.9	4.12	—	3.5	—	
(I_{OH} = 15 mA)				—	—	—	3.94	—	—	—	
(I_{OH} = 20 mA)				3.4	—	3.4	3.70	—	3.0	—	
(I_{OH} = 25 mA)				—	—	—	3.54	—	—	—	
(I_{OH} = 0 mA)			10	9.1	—	9.1	9.58	—	9.1	—	Vdc
(I_{OH} = 5.0 mA)				—	—	—	9.26	—	—	—	
(I_{OH} = 10 mA)				9.0	—	9.0	9.17	—	8.6	—	
(I_{OH} = 15 mA)				—	—	—	9.04	—	—	—	
(I_{OH} = 20 mA)				8.6	—	8.6	8.90	—	8.2	—	
(I_{OH} = 25 mA)				—	—	—	8.70	—	—	—	
(I_{OH} = 0 mA)			15	14.1	—	14.1	14.59	—	14.1	—	Vdc
(I_{OH} = 5.0 mA)				—	—	—	14.27	—	—	—	
(I_{OH} = 10 mA)				14	—	14	14.18	—	13.6	—	
(I_{OH} = 15 mA)				—	—	—	14.07	—	—	—	
(I_{OH} = 20 mA)				13.6	—	13.6	13.95	—	13.2	—	
(I_{OH} = 25 mA)				—	—	—	13.70	—	—	—	
Output Drive Current		I_{OL}									mAdc
(V_{OL} = 0.4 V)	Sink		5.0	0.64	—	0.51	0.88	—	0.36	—	
(V_{OL} = 0.5 V)			10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 V)			15	4.2	—	3.4	8.8	—	2.4	—	
Input Current		I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance		C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) $V_{in} = 0$ or V_{DD}, $I_{out} = 0$ µA		I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
			10	—	10	—	0.010	10	—	300	
			15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)		I_T	5.0	I_T = (1.9 µA/kHz) f + I_{DD}							µAdc
			10	I_T = (3.8 µA/kHz) f + I_{DD}							
			15	I_T = (5.7 µA/kHz) f + I_{DD}							

#Noise immunity specified for worst–case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

** The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3}\ (C_L - 50)\ V_{DD}f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time t_{TLH} = (0.40 ns/pF) C_L + 20 ns t_{TLH} = (0.25 ns/pF) C_L + 17.5 ns t_{TLH} = (0.20 ns/pF) C_L + 15 ns	t_{TLH}	 5.0 10 15	 — — —	 40 30 25	 80 60 50	ns
Output Fall Time t_{THL} = (1.5 ns/pF) C_L + 50 ns t_{THL} = (0.75 ns/pF) C_L + 37.5 ns t_{THL} = (0.55 ns/pF) C_L + 37.5 ns	t_{THL}	 5.0 10 15	 — — —	 125 75 65	 250 150 130	ns
Data Propagation Delay Time t_{PLH} = (0.40 ns/pF) C_L + 620 ns t_{PLH} = (0.25 ns/pF) C_L + 237.5 ns t_{PLH} = (0.20 ns/pF) C_L + 165 ns	t_{PLH}	 5.0 10 15	 — — —	 640 250 175	 1280 500 350	ns
t_{PHL} = (1.3 ns/pF) C_L + 655 ns t_{PHL} = (0.60 ns/pF) C_L + 260 ns t_{PHL} = (0.35 ns/pF) C_L + 182.5 ns	t_{PHL}	5.0 10 15	— — —	720 290 200	1440 580 400	
$\overline{\text{Blank}}$ Propagation Delay Time t_{PLH} = (0.30 ns/pF) C_L + 585 ns t_{PLH} = (0.25 ns/pF) C_L + 187.5 ns t_{PLH} = (0.15 ns/pF) C_L + 142.5 ns	t_{PLH}	 5.0 I0 15	 — — —	 600 200 150	 750 300 220	ns
t_{PHL} = (0.85 ns/pF) C_L + 442.5 ns t_{PHL} = (0.45 ns/pF) C_L + 177.5 ns t_{PHL} = (0.35 ns/pF) C_L + 142.5 ns	t_{PHL}	5.0 10 15	— — —	485 200 160	970 400 320	
$\overline{\text{Lamp Test}}$ Propagation Delay Time t_{PLH} = (0.45 ns/pF) C_L + 290.5 ns t_{PLH} = (0.25 ns/pF) C_L + 112.5 ns t_{PLH} = (0.20 ns/pF) C_L + 80 ns	t_{PLH}	 5.0 10 15	 — — —	 313 125 90	 625 250 180	ns
t_{PHL} = (1.3 ns/pF) C_L + 248 ns t_{PHL} = (0.45 ns/pF) C_L + 102.5 ns t_{PHL} = (0.35 ns/pF) C_L + 72.5 ns	t_{PHL}	5.0 10 15	— — —	313 125 90	625 250 180	
Setup Time	t_{su}	5.0 10 15	100 40 30	— — —	— — —	ns
Hold Time	t_h	5.0 10 15	60 40 30	— — —	— — —	ns
Latch Enable Pulse Width	t_{WL}	5.0 10 15	520 220 130	260 110 65	— — —	ns

* The formulas given are for the typical characteristics only.

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} are not constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Input LE low, and Inputs D, $\overline{\text{BI}}$ and $\overline{\text{LT}}$ high.
f in respect to a system clock.
All outputs connected to respective C_L loads.

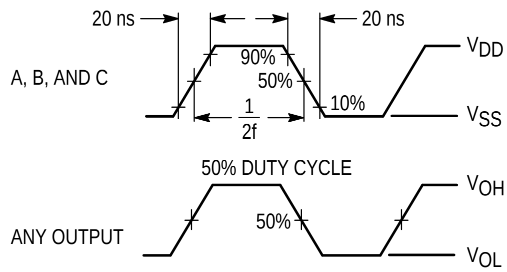
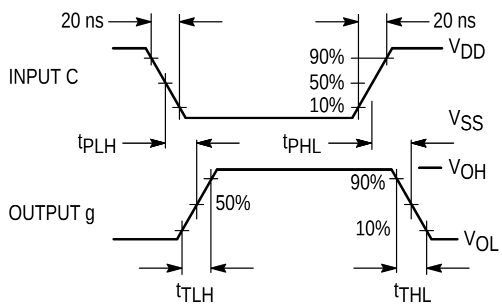
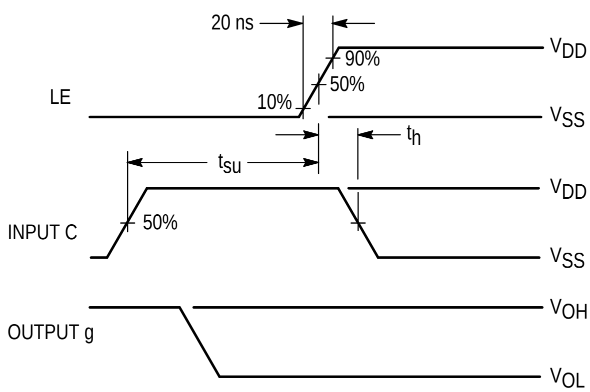


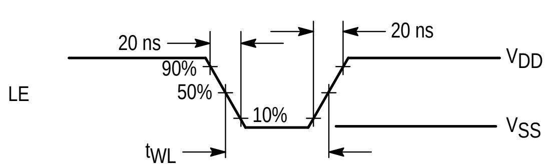
Figure 1. Dynamic Power Dissipation Signal Waveforms



(a) Inputs D and LE low, and Inputs A, B, $\overline{\text{BI}}$ and $\overline{\text{LT}}$ high.



(b) Input D low, Inputs A, B, $\overline{\text{BI}}$ and $\overline{\text{LT}}$ high.

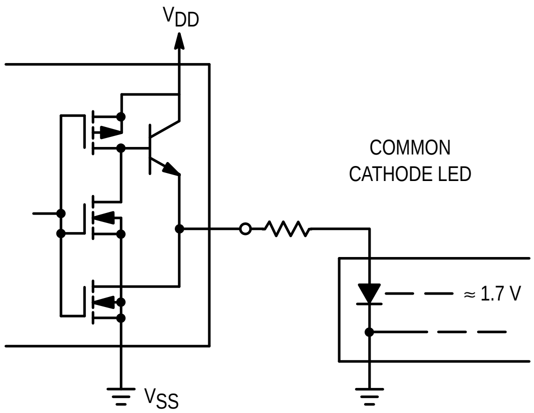


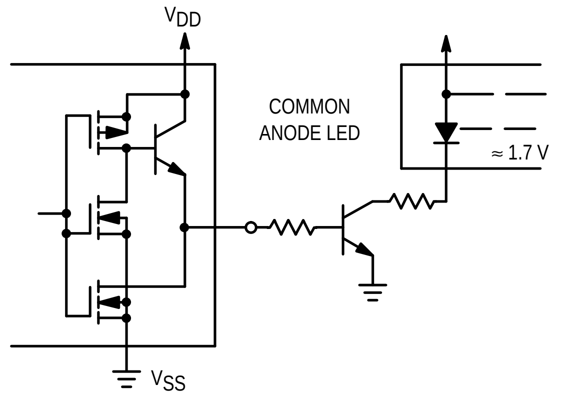
(c) Data DCBA strobed into latches.

Figure 2. Dynamic Signal Waveforms

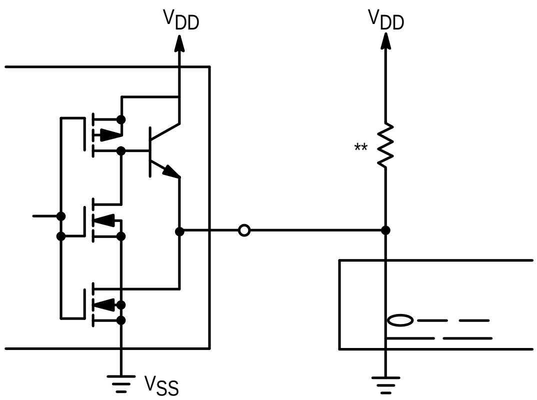
CONNECTIONS TO VARIOUS DISPLAY READOUTS

LIGHT EMITTING DIODE (LED) READOUT

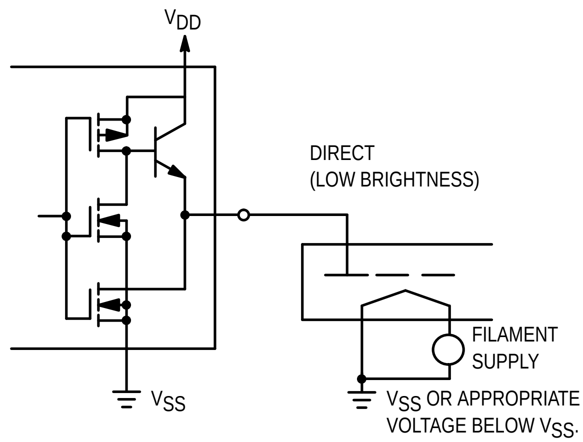




INCANDESCENT READOUT

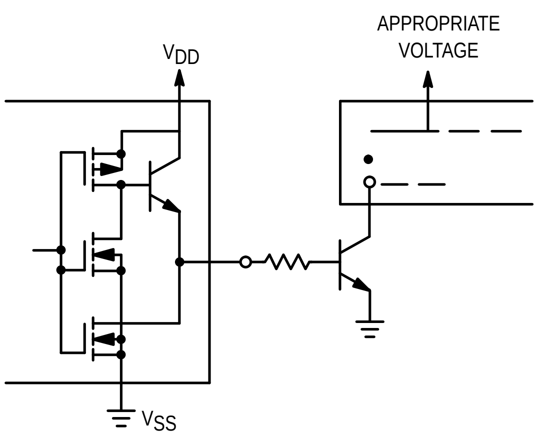


FLUORESCENT READOUT

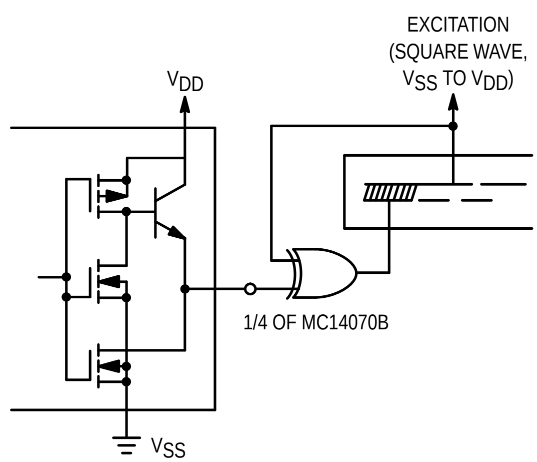


(CAUTION: Maximum working voltage = 18.0 V)

GAS DISCHARGE READOUT



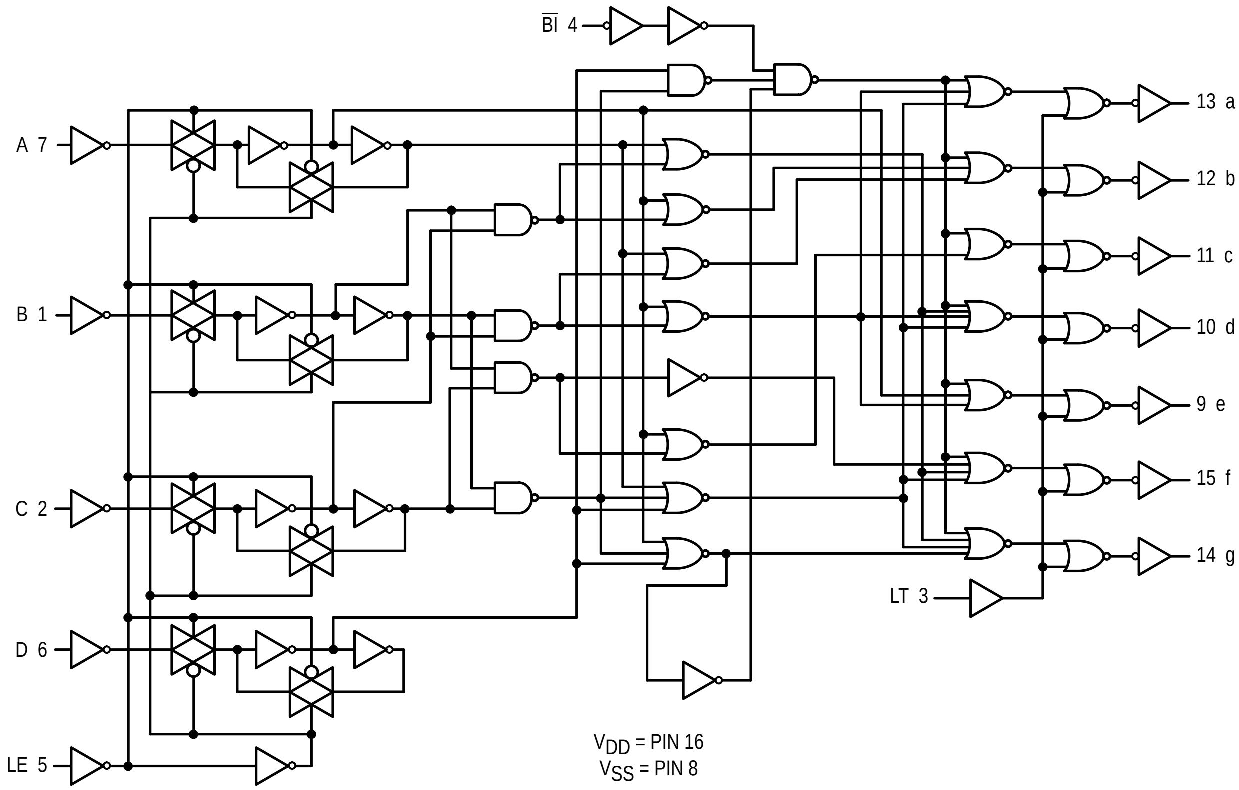
LIQUID CRYSTAL (LCD) READOUT



** A filament pre–warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

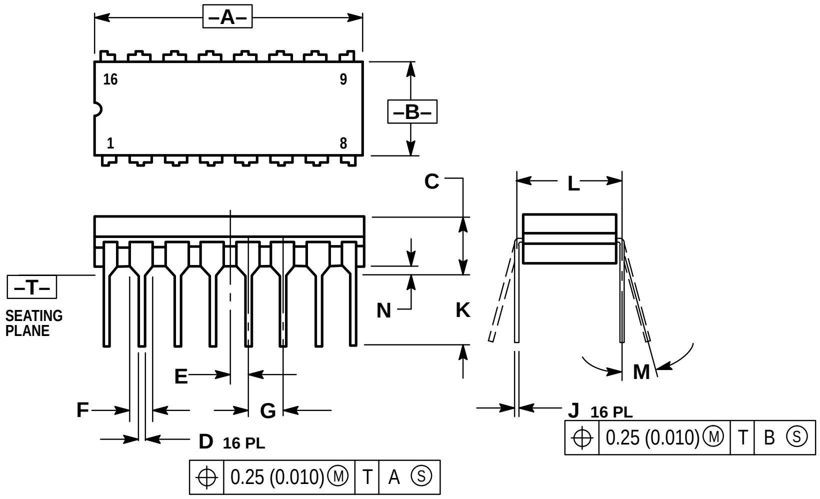
Direct dc drive of LCD's not recommended for life of LCD readouts.

LOGIC DIAGRAM



OUTLINE DIMENSIONS

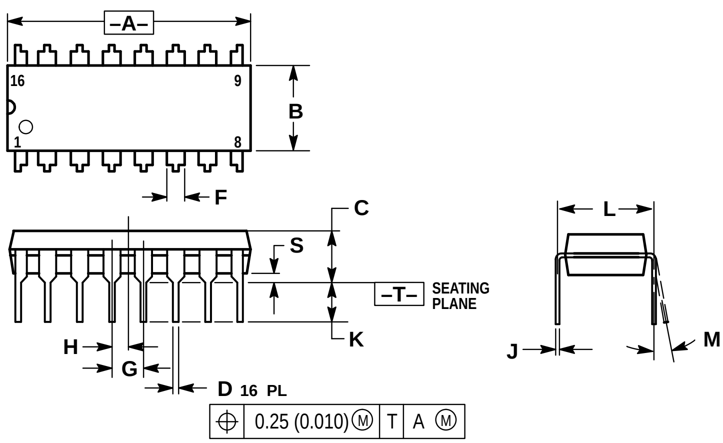
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	---	0.200	---	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

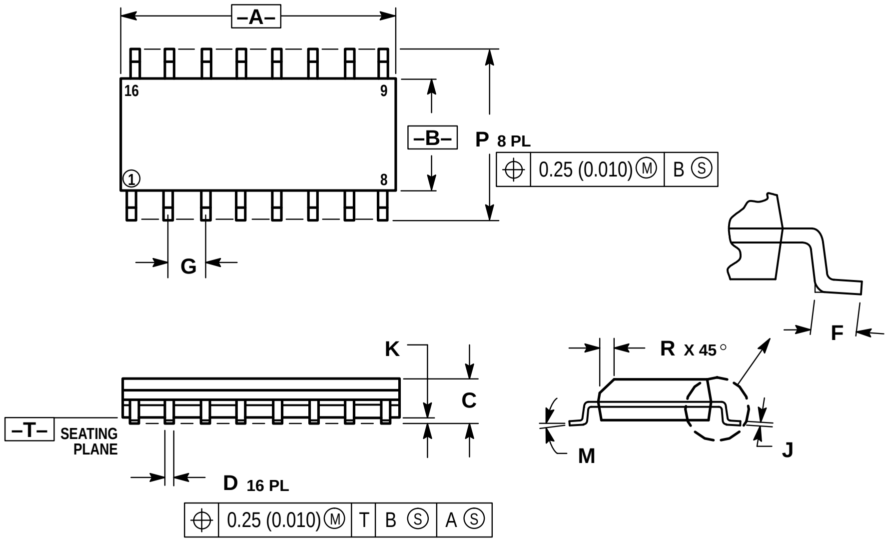


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

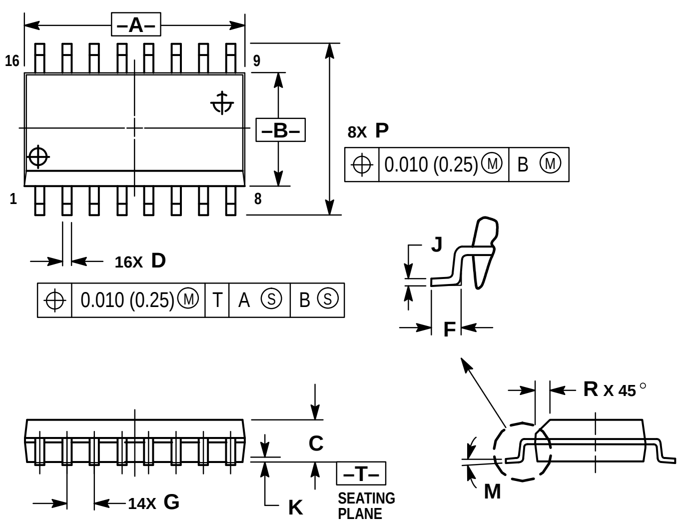
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751G–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

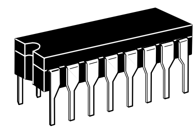
ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

MC14028B

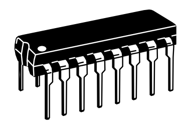
BCD-To-Decimal Decoder
Binary-To-Octal Decoder

The MC14028B decoder is constructed so that an 8421 BCD code on the four inputs provides a decimal (one–of–ten) decoded output, while a 3–bit binary input provides a decoded octal (one–of–eight) code output with D forced to a logic "0". Expanded decoding such as binary–to–hexadecimal (one–of–16), etc., can be achieved by using other MC14028B devices. The part is useful for code conversion, address decoding, memory selection control, demultiplexing, or readout decoding.

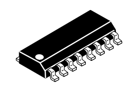
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–power TTL Loads or One Low–power Schottky TTL Load Over the Rated Temperature Range
- Positive Logic Design
- Low Outputs on All Illegal Input Combinations
- Similar to CD4028B.



L SUFFIX
CERAMIC
CASE 620



P SUFFIX
PLASTIC
CASE 648



D SUFFIX
SOIC
CASE 751B

ORDERING INFORMATION

MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBD	SOIC

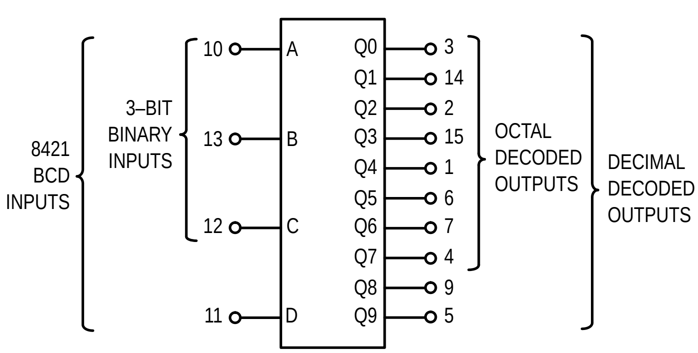
T_A = – 55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	± 10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

BLOCK DIAGRAM



V_{DD} = PIN 16
V_{SS} = PIN 8

TRUTH TABLE

D	C	B	A	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	0	0	0	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	1	0	0	0	0
0	1	0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	1	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

REV 3
1/94

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	— — —	0.05 0.05 0.05	— — —	0 0 0	0.05 0.05 0.05	— — —	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	— — —	4.95 9.95 14.95	5.0 10 15	— — —	4.95 9.95 14.95	— — —	Vdc
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0 10 15	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0 10 15	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0 5.0 10 15	– 3.0 – 0.64 – 1.6 – 4.2	— — — —	– 2.4 – 0.51 – 1.3 – 3.4	– 4.2 – 0.88 – 2.25 – 8.8	— — — —	– 1.7 – 0.36 – 0.9 – 2.4	— — — —	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	0.64 1.6 4.2	— — —	0.51 1.3 3.4	0.88 2.25 8.8	— — —	0.36 0.9 2.4	— — —	mAdc
Input Current	I_{in}	15	—	± 0.1	—	±0.00001	± 0.1	—	± 1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package)	I_{DD}	5.0 10 15	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	µAdc
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (0.3 µA/kHz) f + I_{DD} I_T = (0.6 µA/kHz) f + I_{DD} I_T = (0.9 µA/kHz) f + I_{DD}							µAdc

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

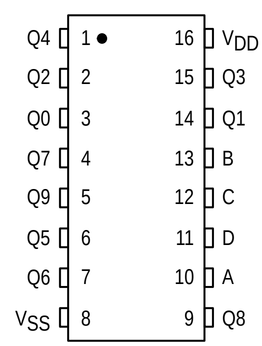
$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	—	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	—	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	—	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns		15	—	90	180	

* The formulas given are for the typical characteristics only at 25°C.
#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

Inputs B, C, and D switching in respect to a BCD code.

All outputs connected to respective C_L loads. f in respect to a system clock.

Inputs A, B, and D low.

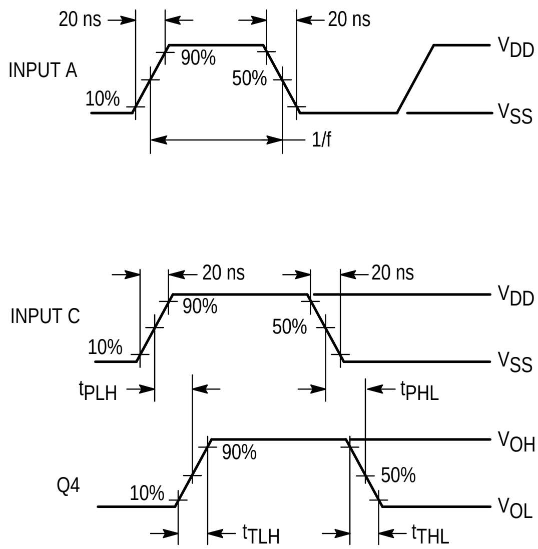
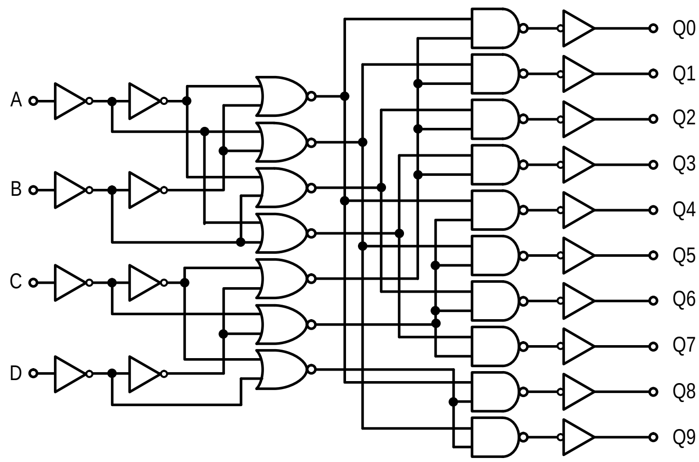


Figure 1. Dynamic Signal Waveforms

LOGIC DIAGRAM



APPLICATIONS INFORMATION

Expanded decoding can be performed by using the MC14028B and other CMOS Integrated Circuits. The circuit in Figure 2 converts any 4–bit code to a decimal or hexadecimal code. The accompanying table shows the input binary combinations, the associated "output numbers" that go "high" when selected, and the "redefined output numbers" needed for the proper code. For example: For the combination DCBA = 0111 the output number 7 is redefined for the 4–bit binary, 4–bit gray, excess–3, or excess–3 gray codes as 7, 5, 4, or 2, respectively. Figure 3 shows a 6–bit binary 1–of–64 decoder using nine MC14028B circuits and two MC14069UB inverters.

The MC14028B can be used in decimal digit displays, such as, neon readouts or incandescent projection indicators as shown in Figure 4.

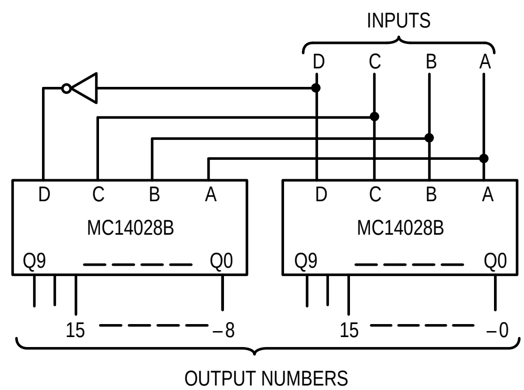


Figure 2. Code Conversion Circuit and Truth Table

Inputs				Output Numbers																Code and Redefined Output Numbers					
																				Hexadecimal		Decimal			
D	C	B	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	4–Bit Binary	4–Bit Gray	Excess–3	Excess–3 Gray	Aiken	4221
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0			0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1			1	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	2	3		0	2	2
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	3	2	0	3	3	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	4	7	1	4	4	
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	5	6	2			3
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	6	4	3	1		4
0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	7	5	4	2		
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	8	15	5			
1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	9	14	6			5
1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	10	12	7	9		6
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	11	13	8		5	
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	12	8	9	5	6	
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	13	9		6	7	7
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	14	11		8	8	8
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	15	10		7	9	9

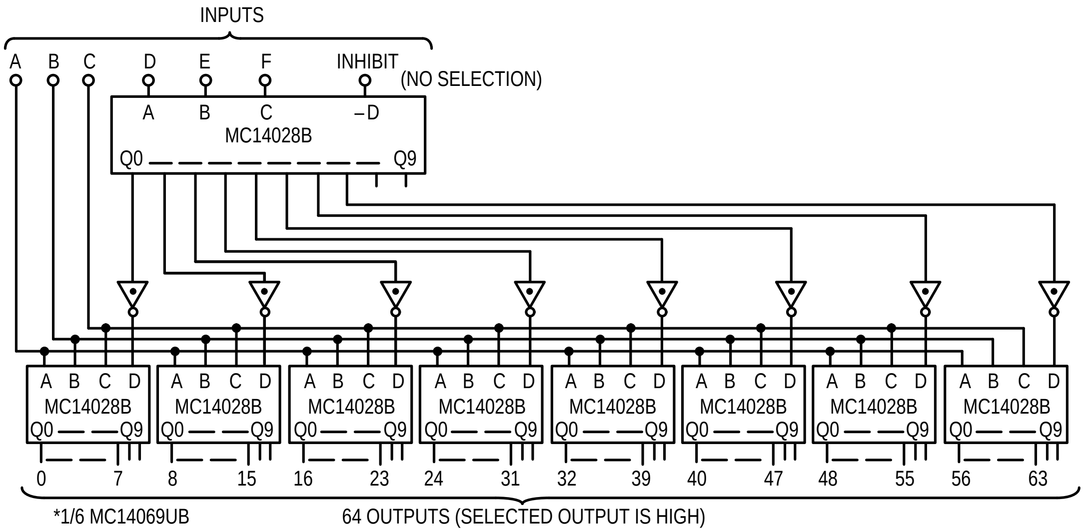


Figure 3. Six–Bit Binary 1–of–64 Decoder

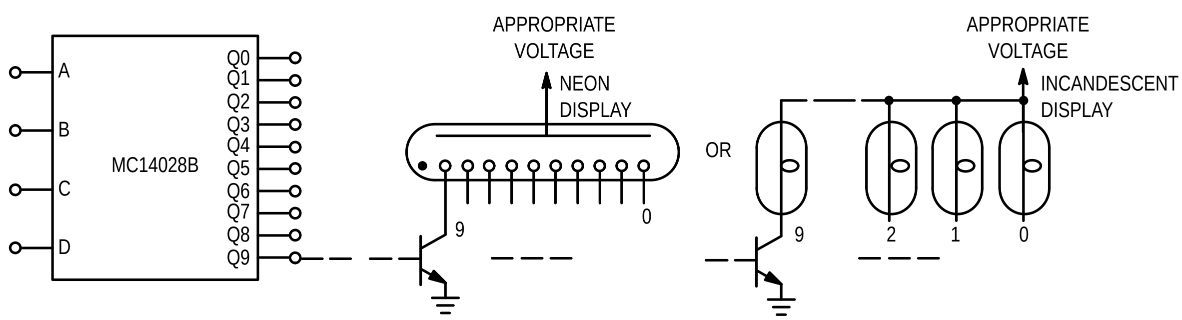
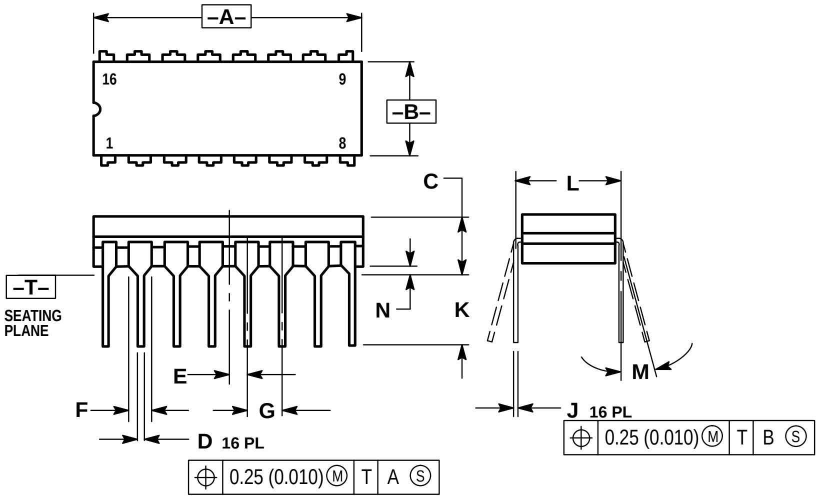


Figure 4. Decimal Digit Display Application

OUTLINE DIMENSIONS

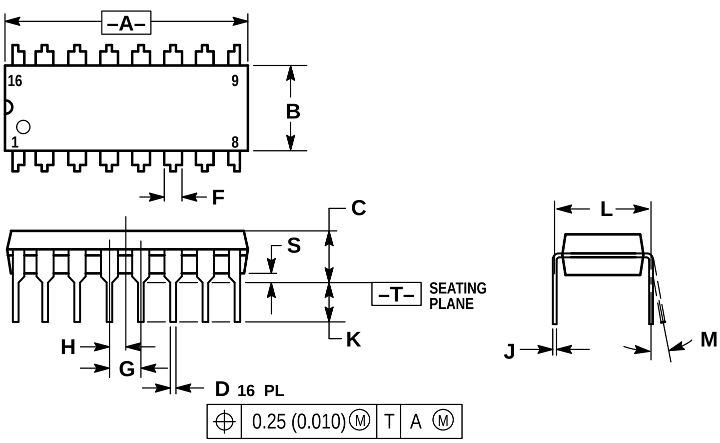
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

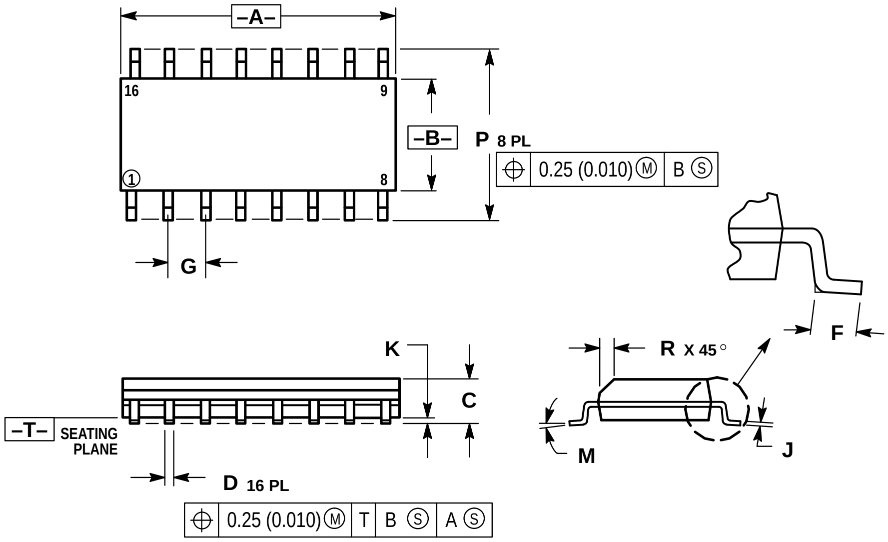


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298